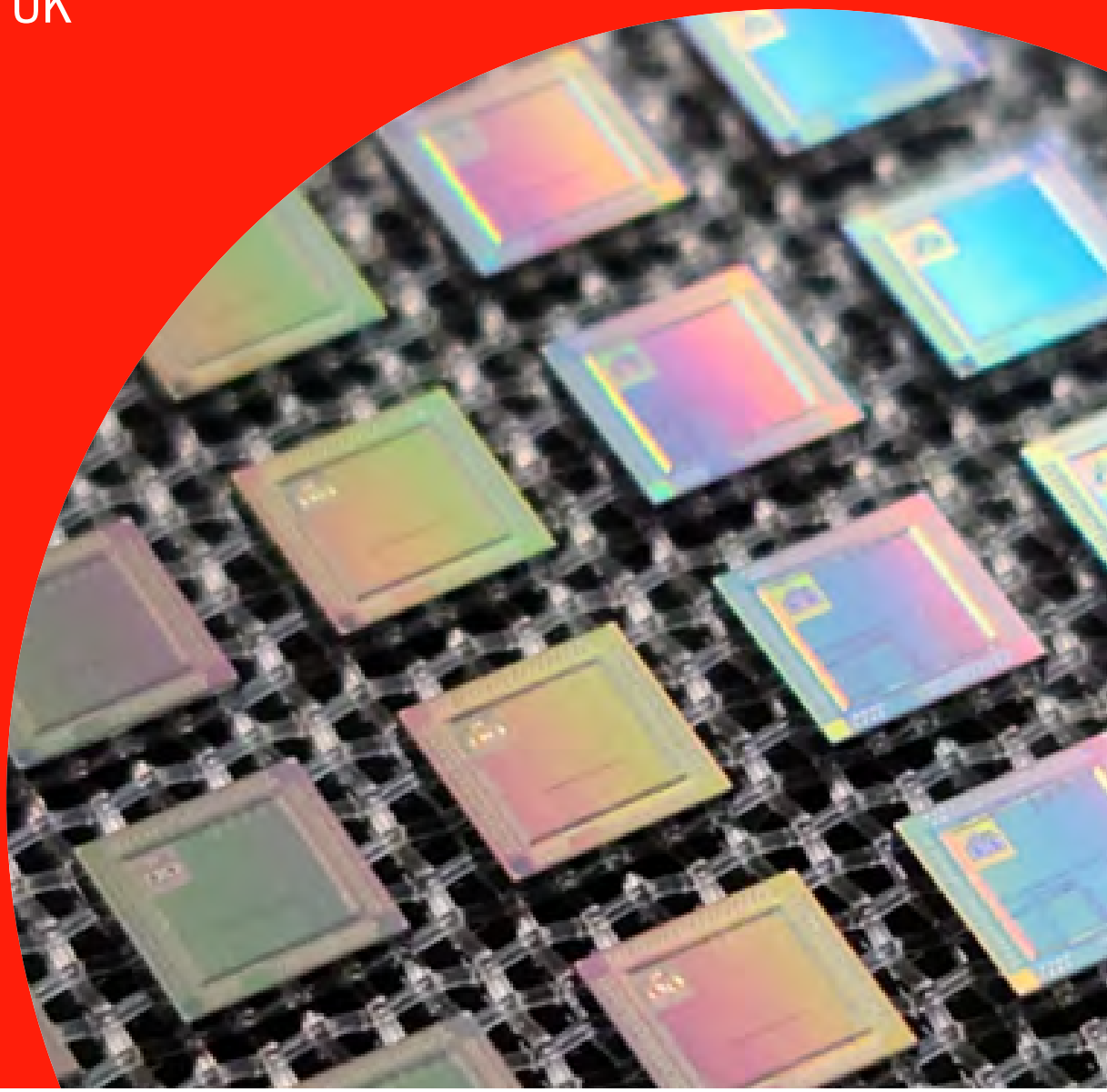
Silicon Quantum Information Processing Workshop 2024

19 September 2024
National Physical Laboratory,
Teddington, UK



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Welcome

On behalf of the organising committee of Silicon Quantum Information Processing (SQIP) 2024, we are delighted to welcome you to this year's conference. This meeting brings together leading researchers from the QIP communities of silicon and related semiconductors, as well as cryo-CMOS designers and engineers who are working at different layers of the "quantum stack".

Information for Speakers

Invited speakers will have 30 minutes (including Q&A), and contributing presenters are given 20 minutes (including Q&A).

We would kindly ask that all presenters arrive in the break before their session and introduce themselves to test their presentation.

Supporting Organisations

We would like to thank the following organisations for their generosity in supporting this event:

NPL National Physical Laboratory

QUANTUM MOTION

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Programme

9:15 AM - 10:00 AM	Arrival and Refreshments
10:00 AM - 10:10 AM	Introduction
10:10 AM - 10:40 AM	**Invited Talk** **Status and perspective of conveyor-mode single electron shuttling in Si/SiGe** Lars R Schreiber (JARA-FIT Institute for Quantum Information)
10:40 AM - 11:00 AM	**The Effective Multivalley Mass Approximation: Simulating the Valley Degree of Freedom in Electron Shuttling** Christian Binder
11:00 AM - 11:20 AM	**Measurement-based quantum computing with arsenic dopants in silicon** Mr Matthew Tam
11:20 AM - 11:50 AM	Morning Coffee/Tea Break
11:50 AM - 12:20 PM	**Invited Talk** **A multi-module silicon-on-insulator chip assembly containing quantum dots and cryogenic radio-frequency readout electronics** Alberto Gomez-Saiz (Quantum Motion Technologies)
12:20 PM - 12:40 PM	**Ultra-low power cryo-CMOS for interfacing quantum processors** Janne Lehtinen
12:40 PM - 1:00 PM	**Efficient large-scale cryogenic CMOS characterization** Jonathan Eastoe
1:00 PM - 2:00 PM	Lunch and Posters
2:00 PM - 2:30 PM	**Invited Talk** **Superconductor-semiconductor hybrid circuits on a germanium 2DEG platform** Anasua Chatterjee (Niels Bohr Institute, University of Copenhagen)
2:30 PM - 2:50 PM	**QDsim: A user-friendly toolbox for simulating large-scale quantum dot devices** Vinicius Hernandes
2:50 PM - 3:10 PM	**SQUADs: A Radiofrequency (RF) Reflectometry Simulator for Quantum Dot Arrays** Tara Murphy
3:10 PM - 3:30 PM	Afternoon Coffee/Tea Break

3:30 PM - 4:00 PM	**Invited Talk** **Quantum system on a chip architecture and design detail challenges** David Redmond (Equal1 Laboratories Ireland, University College Dublin)
4:00 PM - 4:20 PM	**Resistive memory devices at cryogenic temperatures for quantum technologies** Gokhan Bakan
4:20 PM - 4:40 PM	**Spin polarimetry in the solid state** Lorenzo Peri
4:40 PM - 5:00 PM	**Closing Remarks**
5:00 PM - 6:00 PM	**Lab Tour and Walk to Dinner Venue (AQML)**
6:00 PM - 8:00 PM	**Dinner and Drinks Reception (AQML)**

Oral Presentations

A multi-module silicon-on-insulator chip assembly containing quantum dots and cryogenic radio-frequency readout electronics

Gomez-Saiz A

Quantum processing units will be modules of larger information processing systems containing also digital and analog electronics modules. Silicon-based quantum computing offers the enticing opportunity to manufacture all the modules using the same technology platform. Here, we present a cryogenic multi-module assembly for multiplexed readout of silicon quantum devices where all modules have been fabricated using the same fully-depleted silicon-on-insulator (FDSOI) CMOS process. The assembly is constituted by three chiplets: (i) a low-noise amplifier (LNA), (ii) a single-pole eight-throw switch (SP8T), and (iii) a silicon quantum dot (QD) array. We characterise each module individually and show (i) a gain over 35 dB, a bandwidth of 118 MHz, a minimum noise temperature of 4.2 K, (ii) an insertion loss smaller than 1.1 dB, a noise temperature smaller than 1.1 K across 0-2 GHz, and (iii) single-electron box (SEB) charge sensors. Finally, we combine all elements into a single demonstration showing time-domain radio-frequency multiplexing of two SEBs paving the way to an all-silicon quantum computing system.

Quantum system on a chip architecture and design detail challenges

Redmond D

Building a fully integrated QSoC builds on 50 years of semiconductor technology evolution, and offers a bright roadmap for large scale high performance qubits that have potential for wide range of applications. However the design and implementation details pushes the envelope of current circuits, and SoC architectures, requiring alternate approaches and architectural. I will discuss a variety of these new engineering challenges and some novel solutions useful for silicon spin qubits.

Superconductor-semiconductor hybrid circuits on a germanium 2DEG platform

Chatterjee A

Hole spin qubits in strained planar germanium quantum wells (Ge/SiGe) have emerged as a promising qubit candidate for quantum information processing and simulation. Recently, hard-gapped superconductivity has been engineered for the first time in Ge/SiGe, in a wide range of mesoscopic devices. The demonstration of an isotopically purifiable semiconductor platform that can host clean superconductivity places Ge/SiGe in a uniquely advantageous position, facilitating many opportunities for hybrid superconducting-semiconducting quantum dots, including high fidelity two-qubit gates, extended range qubit-qubit coupling without the need for resonators, and integration with circuit QED. I will describe our progress toward these goals.

Efficient large-scale cryogenic CMOS characterization

Eastoe J, Noah G, Dutta D, Rossi A, Fletcher J, Gómez Saiz A

Enhancing scalability is one of the primary challenges currently being faced in the quantum computing community. The migration of the classical electronics facilitating the control and readout of individual qubits into the cryostat is a key milestone in this endeavor. Integrating the electronics, either on chip or an intermediate temperature stage, will diminish the reliance on numerous analogue connections between room temperature and sub kelvin components.

Developing such cryogenic hardware in silicon, using foundry fabricated CMOS transistor technology would allow the utilization of standard foundry processes and decades of established knowledge. Extending process design kits, needed to understand the performance and variability of the transistors that will form the building block of any complex cryogenic hardware requires the meticulous characterization of a large number of transistors across numerous geometries.

Due to the quantity of devices that must be characterized, individually bonding transistors for testing is not viable. Testing devices via a cryogenic probe station is efficient in terms of both testing time and utilization of surface area on test wafers, however the hardware necessary is expensive. In this work we discuss the development of a cryogenic test system using integrated on-die multiplexers to efficiently characterize thousands of transistors in a liquid helium dipping station. The test system was utilized to characterize thousands of transistors across multiple dies, allowing the statistical spread of key attributes such as threshold voltage and on current to be measured as a function of device geometry, wafer position and inter die variation.

Measurement-based quantum computing with arsenic dopants in silicon

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Dopants in silicon have demonstrated exceptionally long coherence times and can benefit from the scalability of silicon-based nano-electronic processes. Arsenic dopants also benefit from a 3/2 nuclear spin manifold, allowing qudit encoding on the nuclear spins.

We demonstrate the fabrication of arsenic dopants with atomic-scale precision as quantum dots and SETs on a silicon substrate and the characterisation of DC transport and RF reflectometry on these devices. Our RF reflectometry measurements use variable capacitors (varactors) to impedance match RLC circuits connected to the qubits to the transmission lines, which allows us to match the quantum capacitance associated with the spin state to the reflection coefficient of the RF signals.

We also lay down the theory for a measurement-based entanglement scheme between remotely separate spin qubits. Entangling measurements arise from multi-qubit measurements where there is indistinguishability between the qubits the measurement is performed over. Previously demonstrated for superconducting qubits, measurement-based entanglements also open the door to all-to-all connectivity between qubits, overcoming the nearest-neighbour limitation for conventional two-qubit gates and allowing the creation of a measurement-based universal quantum computer.

QDsim: A user-friendly toolbox for simulating large-scale quantum dot devices

Hernandes V[1], Gualtieri V[1], Renshaw-Whitman C[1], Greplova E[1]
[1]Delft University Of Technology

Quantum dots (QDs) have emerged as a particularly promising quantum computing platform. These semiconducting systems confine charge carriers within potential wells, or “dots”, leveraging well-established semiconductor fabrication techniques. The scalability of QD-based qubits is crucial for practical quantum computation. However, as device sizes increase, manually tuning each quantum dot becomes unfeasible, pushing the need for automated systems. Artificial intelligence (AI) presents a viable solution, offering the potential to learn and dynamically adjust to the complex behavior of quantum dots. However, effective AI applications require extensive datasets that accurately represent the varied operational regimes of quantum dot arrays. The shortage of such data significantly impedes progress in the field.

To address these challenges, we introduce QDsim, a Python-based computational framework that simplifies the simulation of quantum dot arrays into a convex optimization task. This toolbox, which operates under the constant interaction model, is designed to expedite the generation of charge stability diagrams—crucial tools for visualizing the relationship between gate voltages and charge configurations.

QDsim surpasses existing simulators by offering unprecedented flexibility in device geometry, allowing for the customized placement of dots, gates, and sensors. Additionally, QDsim’s ability to generate diagrams for systems with over 100 quantum dots in less than 4 minutes marks a significant advancement in the field. By producing large-scale, relevant datasets, QDsim serves as an essential tool for training machine learning models that automate quantum device tuning, setting the stage for future AI-driven automatization in quantum device management.

Resistive memory devices at cryogenic temperatures for quantum technologies

Bakan G

Memory devices enable modern computing by storing information as bits. They are either volatile, i.e., data is lost when power is cut, like SRAM and DRAM or they are non-volatile like magnetic or flash memory. Although the charged-based flash memory dominates the non-volatile memory market (e.g., SSDs), their shortcomings invited developments of other technologies like phase-change and resistive memory devices. While the primary objective of such emerging non-volatile memory technologies is to replace the dominant technology or find a niche position in the memory hierarchy, they have actively supported the activities in the neuromorphic field which employs such devices as pseudo-synapses whose plasticity (electrical resistances) can be modified by potentiation or depression (decreasing or increasing the resistance) [1]. The promise of low-power consumption of neuromorphic computation makes it especially appealing for the functions of classical computing in quantum technologies due to the low thermal budget requirement at cryogenic temperatures. In this presentation, we will show our results on SiOx resistive memory devices operating at cryogenic temperatures. The results will include the device stability in high and low resistance states and how to improve the device behaviour. Furthermore, we demonstrated that they can operate, i.e., transition between high and low resistance states with appropriate electrical signals, in the temperature range of 2 K to 300 K. This is a crucial step towards achieving low-power alternative computing at cryogenic temperatures supporting the quantum computing applications.

[1] Sangwan, V.K., Hersam, M.C., Nat. Nanotechnol. 15, 517–528 (2020).

Spin polarimetry in the solid state

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[1]University Of Cambridge, [2]Quantum Motion, [3]Institute of Physics, University of Augsburg

Spins confined in semiconductor quantum dots (QDs) are promising candidates for quantum information processing. These systems are subject to spin-orbit coupling (SOC), which causes increased qubit variability but offers the enticing opportunity for all-electrical control, generating growing interest in hole-based architectures. However, the presence of SOC inevitably poses challenges. Particularly, for spin readout, it may lift Pauli spin-blockade (PSB) many readout schemes rely upon.

We shed light, experimentally and theoretically, on the problem of spin-projective measurements in double QDs subject to SOC. We recast the dynamics of this system in terms of the simpler behaviour of a single spin travelling through an active medium, a process akin to photon polarimetry. By reframing the problem, we provide new insight on well-known concepts such as g-tensors misalignment, spin-conserving, and spin-flip tunnel couplings, offering a geometrical interpretation for SOC-induced avoided crossings and emphasising the conditions to avoid PSB lifting.

We explore these concepts experimentally using a spin-orbit-coupled double QD, realised as a gate-defined QD tunnel-coupled to a Boron acceptor in a p-type silicon nanowire FET (a-b). We perform the single-spin equivalent of optical polarimetry by adiabatically connecting the (1,1) spin ground-state and the (0,2) spin-singlet of the Boron while monitoring the radio-frequency reflectometry signal for changing magnetic field direction (c-d).

From the geometry behind PSB and its lifting arises a simple picture of how the blockade is modified by the presence of SOC, naturally leading to a figure of merit: the maximum achievable readout fidelity, quantifiable in terms of experimentally measurable device parameters such as g-tensor misalignment, and direction and magnitude of spin-flip tunnelling. This work poses a fundamental upper bound on PSB readout in the (inevitable) presence of SOC, acting as a cautionary tale for future QD quantum-computing architectures, particularly hole-based, and highlighting which parameters to focus on to mitigate its effect.

SQUADs: A Radiofrequency (RF) Reflectometry Simulator for Quantum Dot Arrays

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Spins in semiconductor quantum dots represent a very large-scale integration route for quantum computing hardware. Many efforts have been devoted to creating quantum dot array simulators, with an aim to better understand the complexity of these systems as they scale up. Typically based on the well-established Constant Interaction Model (CIM), which provides a good starting point for understanding these systems, it fails to explain important experimental details, such as the set up used to measure the device.

We present a physics-based quantum dot array simulator capable of realistically replicating the outputs of radiofrequency reflectometry measurements. Implemented in JAX, an accelerated linear algebra library, our simulator facilitates the generation of large, realistic datasets, resolving a double quantum dot with maximum occupancy of ten electrons in each dot in 1.4ms at the CIM level.

A key feature of our simulator is the inclusion of advanced physical phenomena. The use of tunnel couplings, the use of the WKB approximation, Fock-Darwin states and different noise models in our simulation are all essential for accurately capturing the behaviour of quantum dots in experimental conditions. Furthermore, our simulator supports device plotting capabilities, enabling users to visualise their quantum dot arrangements and sensor placements directly.

The core objective of our work is to deliver a simulator that is powerful, easy to use, accessible, and open source. We aim to provide experimentalists with a tool that is well-documented and accompanied by a set of examples and tutorials, making it straightforward to adopt and apply to various research scenarios.

Status and perspective of conveyor-mode single electron shuttling in Si/SiGe

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Long-range coherent qubit coupling is a missing functional block for a scalable architecture of a spin-qubit based quantum computer. In a conveyor-mode shuttle, the spin-qubit is adiabatically transported while confined to a propagating sinusoidal potential in a gate-defined quantum channel [1]. Its key feature is the all-electrical operation by only few easily tunable input terminals.

In this talk, I discuss progress on conveyor-mode single electron shuttling in Si/SiGe [2]. In a 10 µm long shuttle device, we experimentally demonstrate a shuttle fidelity of 99.7±0.3% across the full device and back with a total distance of 19 µm as well as shuttle-based charge initialization of 34 quantum dots [3]. Raising the shuttle velocity to 2.8 m/s, we observe spin coherent shuttling by separation and rejoining of a spin EPR pair [4]. The shuttle process is sensitive to electrostatic disorder and local variations of the valley splitting. This in turn facilitates the two-dimensional mapping of local material properties such as the valley splitting [5]. Ultimately, spin-coherent conveyor-mode electron-shuttling in conjunction with T-junctions could enable two-dimensional sparse qubit-architecture hosting millions of spin-qubits [6,7].

[1] Langrock, Krzywda ea. PRX Quantum 4, 020305 (2023).
[2] De Smet ea., arXiv:2406.07267 (2024).
[3] Xue ea. Nat. Commun. 15, 2296 (2024).
[4] Struck ea. Nat. Commun. 15, 1325 (2024).
[5] Volmer, ea. npj Quantum Inf. 10, 61 (2024).
[6] Boter ea. Phys. Rev. Appl. 18, 024053 (2022).
[7] M. Kuenne ea. Nat. Commun. 15, 4977 (2024).

The Effective Multivalley Mass Approximation: Simulating the Valley Degree of Freedom in Electron Shuttling

Binder C

Electron shuttling is a key technique for advancing quantum computing, offering reliable electron transfer over long distances with minimal charge loss. Recent studies have shown that motionally induced spin flip errors are negligible, shifting the primary concern to phase errors caused by positionand valley-dependent g-factors. These phase errors become particularly significant at the high velocities required for rapid quantum operations, posing a challenge to achieving the high fidelities necessary for error correction schemes. Notably, the valley-dependent g-factor variation remains inadequately addressed by existing analytical methods, which cannot fully capture the complexities of an electron shuttled along a rough surface.

In this talk, we address this critical gap by developing a novel, fast, and stable numerical approach to study electron shuttling, accurately capturing the essential physics of the valley degree of freedom in both time-dependent and time-independent contexts. This approach overcomes the limitations of current analytical methods and provides a comprehensive tool for understanding the time-evolution of the valley-orbit electronic wavefunction during shuttling. Our method significantly enhances the understanding of electron shuttling dynamics and might hence contribute to the efforts of mitigating shuttling-induced phase errors. We validate our approach through rigorous cross-benchmarking between numerical and analytical techniques and tackle a variety of valley-induced problems.

Specifically, we investigate the impact of surface roughness on the excitation of the valley degree of freedom during shuttling, the influence of quantum dot size on these excitations, and the effects of noise-induced trajectory variations on phase errors. This work represents a crucial step toward enabling the high-speed, high-fidelity shuttling necessary for large-scale quantum computing.

Ultra-low power cryo-CMOS for interfacing quantum processors

Lehtinen J

Low temperature CMOS, so-called cryo-CMOS, has been investigated and utilized widely for various cryo-enabled applications. Recently, the rise of quantum technologies has increased the demand of high performance cryo-electronics, especially, for interfacing solid-state quantum processors and the field has turned its attention towards cryo-CMOS [1,2]. We use our in-house FDSOI technology (~20 nm thick Si channel) to fabricate the quantum dots and CMOS circuits on the same wafer [3]. The QDs are defined by Si mesa geometry and two layers of gates.

One of the most limiting factor for practical low-dissipation cryogenic CMOS devices has been the switching efficiency. It has been significantly lower than suggested by thermionic limits, even at temperatures as high as 4 K. Here, we introduce a novel Si MOSFET that is tailored for specifically for cryogenic and quantum computing applications. For the first time ever, we achieve switching efficiency surpassing 1 mV per decade subthreshold swing. In addition, we utilize customized FDSOI technology that enables independent electrostatic tuning of threshold voltages. Together these two factors, the ultra-sharp switching and capability to tune the threshold voltage, enables realization of ultra-low power dissipation logic circuits with only few tens of mVs drive voltages.

[1] B. Patra et al., IEEE J. of Solid-State Circ. 53, 309 (2018). https://doi.org/10.1109/JSSC.2017.2737549
[2] X. Xue et al. Nature 593, 205 (2021). https://doi.org/10.1038/s41586-021-03469-4
[3] H. Bohuslavskyi et al. https://arxiv.org/abs/2208.12131

Posters

Challenging the cryogenic wiring bottleneck with intra-cryostat wireless communication

Barr K

Implementation of qubit technologies for applications in QIP, from gate-defined semiconductor QDs to superconducting qubits and resonators, often require sub-kelvin temperatures to perform effectively. As we increase system complexity, we quickly face a wiring bottleneck [1], whereby the increased interconnections generate heat and noise, degrading qubit fidelities. A solution is required prior to significant progress towards larger, more complex, systems.

Silicon cryo-CMOS technologies reduce wiring through integrated multiplexing and efficient signal routing. Yet Si-CMOS at deep-cryogenic temperatures (≤ 4K) require further advancements to reduce power consumption and self-heating [1,2]. Currently, on-chip heating is still too large if compared with the limited cooling power available in typical dilution refrigerators. An alternative to the problem is to circumvent the wiring entirely. Development of multi-stage, in-fridge wireless technologies [3] offers an alternative that can be integrated alongside cryo-CMOS to improve scaling efforts.

In this work, we present an in-fridge transmitter/receiver μ-wave array-antennas with lenses designed to optimize signal transmission through multiple fridge stages. Blackbody calculations found that the radiated heat can be managed to allow transmission directly from room temperature to mK stages. With the inclusion of transmission windows to manage radiative heat load.

Previous work [4] showed efficient antennas at 77 K, while we have shown initial transmission experiments at 4 K. We now move towards multi-stage wireless transmission from either the RT or 50 K stage directly to mK with an NbN resonator [5] as the initial DUT. After demonstration of wireless with wired readout, we will transition to full wireless in-fridge communication.

[1] Sebastiano, F. et al. Cryo-CMOS Electronic Control for Scalable Quantum Computing: Invited. in Proceedings of the 54th Annual Design Automation Conference 2017 1–6 (ACM, Austin TX USA, 2017). doi:10.1145/3061639.3072948.
[2] X. Xue et al., ‘CMOS-based cryogenic control of silicon quantum circuits’, Nature, vol. 593, no. 7858, pp. 205–210, May 2021, doi: 10.1038/s41586-021-03469-4.
[3] J. Wang et al., ‘34.1 THz Cryo-CMOS Backscatter Transceiver: A Contactless 4 Kelvin-300 Kelvin Data Interface’, in 2023 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA: IEEE, Feb. 2023, pp. 504–506. doi: 10.1109/ISSCC42615.2023.10067445.
[4] Rehman Kazim, J. ur et al. Wireless Microwave Signal Transmission for Cryogenic Applications. in 2023 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (USNC-URSI) 43–44 (2023). doi:10.1109/USNC-URSI52151.2023.10237549.
[5] Foshat, P. et al. Characterizing Niobium Nitride Superconducting Microwave Coplanar Waveguide Resonator Array for Circuit Quantum Electrodynamics in Extreme Conditions. Preprint at https://doi.org/10.48550/arXiv.2306.02356 (2023).

EQUINOX, IUK project

Hall S

Quantum scalable networks for secure communication, advanced sensing and distributed quantum computing require a robust eco-system of optical and photonic building blocks at the physical layer to assemble distributed and scalable quantum interconnect networks.

To allow the distribution and processing of qubits in the form of entangled photons and single photons EQUINOX will develop a suite of critical physical layer building blocks at the quantum fabric, board and chip level. EQUINOX will also develop new metrology schemes for quantum fidelity of physical layer interconnect components and prepare the first international standards for quantum interconnect through the IEC TC86 and the newly established UK managed IEC-ISO Joint Technical Committee on Quantum Technologies.

The EQUINOX consortium spans a UK value chain suitable to deliver quantum subsystem development, interconnection, metrology and validation in hyperscale data centres, HPC and 5G environments, thus underpinning the UK's place as the world-leader in the future quantum network ecosystem.

EQUINOX will help establish an extended UK quantum supply chain, empowering the UK and international customers, both small and large, to access UK quantum goods and services by supplying validated performance characteristics for 2nd generation quantum network technologies.

Low Temperature SOLR Calibration for Precise S-Parameter Measurements of Quantum Devices

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Accurate RF measurements at low temperatures are essential for understanding the behaviour of superconducting devices. Achieving such precision requires accounting for phase changes and losses introduced by components in the cryogenic environment, such as cables, interconnects, amplifiers, and attenuators.

This precision is achieved by moving the calibration reference plane from the VNA level at room temperature to the cryogenic base temperature, as close as possible to the Device Under Test (DUT). This involves embedding the SHORT, OPEN, LINE, and Reciprocal THRU (SOLR) standards at millikelvin temperatures, following the same paths as the DUT [1] [2]. This calibrated measurement setup is then installed in a 300 mK He-3 refrigerator for low-temperature, high-accuracy device characterization.

The novelty of this technique lies in its application for in-operando calibration of cryogenic devices, enabling precise characterization of commercial devices such as Josephson Parametric Amplifiers (JPAs) at millikelvin temperatures—critical for advancing quantum computing. The method is compact and simpler to implement than traditional calibration techniques, such as Thru-Reflect-Line (TRL), which are complicated by factors like thermal contraction. This simplicity and adaptability make it suitable for a broad range of cryogenic environments and device types, enhancing the feasibility of advanced low-temperature measurements.

[1] M. Stanley, M. Salter, J. Urbonas, J. Skinner, S. Shin, S. E. De, and N. M. Ridler, "Characterizing S-Parameters of Microwave Coaxial Devices with Up to Four Ports at Temperatures of 3 K and Above for Quantum Computing Applications," IEEE Transactions on Instrumentation and Measurement, vol. 73, pp. 1-6, 2024.
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Microwave on-wafer S-parameter measurements at cryogenic temperatures for quantum computing applications

Shang X[1], Stokes D[1], Manning L[1], Sweetnam T[1], Lindstrom T[1], Ridler N[1]
[1]NPL

The realisation of fully scaled-up quantum computers requires microwave on-wafer S-parameter measurements of planar circuits, such as those used in qubit control and readout systems. With on-wafer measurements, the device under test can be characterised directly at cryogenic temperatures, eliminating the need for additional connectors or interfaces. This paper reports on recent developments in cryogenic on-wafer S-parameter measurements at the National Physical Laboratory (NPL), in collaboration with Royal Holloway, University of London. Specifically, it discusses the adaptation and improvement of a cryogenic probe station for microwave probing (at around 4 kelvin) and the development of bespoke calibration and verification standards based on coplanar waveguide (CPW) structures. An overview of the state-of-the-art will also be provided by reviewing similar work undertaken by other groups. Such cryogenic on-wafer measurement capabilities will help facilitate current and future developments in commercial quantum computers.

On-Chip Microwave Antenna for Silicon Donor Spin Qubit Control

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Donor spin qubits in silicon have been identified as promising candidates for the implementation of a quantum computer. Using scanning tunnelling microscopy (STM) hydrogen-resist lithography, individual donor atoms can be positioned in the silicon lattice with atomic precision and assembled to create planar nanostructures such as single electron transistors (SET), quantum dots, and single donor atom qubits. To effectively manipulate these qubits, accurate control antennas must be integrated within the atomically precise dopant devices. In this work, we explore the design and fabrication of these integrated control antennas. After establishing single electron device characterization, including independent spin-state readout and spin correlation measurements, the next requirement for our donor spin qubit devices is local control of the qubit spin states. This can be achieved by post-fabrication of a microwave antenna on the surface of the donor device chip; an input microwave signal is guided along a transmission line that terminates in a short-circuit loop next to the qubit, producing oscillating magnetic fields to drive qubit spin-state transitions. The challenges facing antenna implementation involve balancing the requirements of impedance matching with antenna layout and materials processing parameters and achieving high accuracy alignment. We address these challenges using CST suite simulation results, and by developing an alignment process using kelvin probe force microscopy (KPFM) to map donor device structures and subsequently transfer antenna patterns by electron beam lithography (EBL) to within 100s of nanometres of the target qubit. We discuss these results and ongoing work work with design and fabrication of the antennas.

Using TCAD simulations for exploring quantum dot formation in industry compatible Fully Depleted Silicon-On-Insulator transistors

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[1]Department of Physics, SUPA, University of Strathclyde, [2]National Physical Laboratory

Silicon nanostructures, such as metal oxide semiconductor field effect transistors (MOSFETs) mass produced by commercial foundries, have recently emerged as contenders for trapping single electrons that can be used for quantum dot arrays [1]. Some silicon technologies, like fully depleted silicon-on-insulator (FDSOI), lend themselves particularly well to creating quantum dots (QDs) due to their geometric features, like ultra-thin silicon channels, and tuneable electric fields [2].

To extract the electric field, charge carrier density, and band structure inside of MOSFETs, a simulation tool, Sentaurus Technology Computer Aided Design (TCAD), was used [3,4]. From the band structure, well-known Schrodinger equation solutions (harmonic oscillator and infinite potential well) were fitted to the conduction band edge to find the energy state separation. Finally, Coulomb blockade energy was estimated via the QD dimensions and parallel plate capacitance.

We simulate MOSFETs realised in a commercial 22nm FDSOI node for different gate arrangements. First, a traditional single-gate MOSFET, that has been shown to trap electrons experimentally [5], was simulated and revealed several ways QDs can form. Interestingly, these included QDs forming near the edge of the transistor channel by accumulating carriers between trench isolation regions and the Si/Oxide interface. Next, a 3-gate MOSFET that allows easily controllable QDs to be generated by using selected gates to define variable confinement barriers. The energy state separation and Coulomb blockade suggest these MOSFETs can operate as single spin qubits at mK temperatures.

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[2] I. Kriekouki et al. Solid-State Electronics, 204, 108626 (2023)
[3] F. A. Mohiyaddin et al. IEEE, IEDM, 39.5-39.4 (2019)
[4] F. A. Mohiyaddin et al. IEEE, SISPAD, 253-256 (2023)
[5] E. J. Thomas et al. arXiv:2310.20434 (2023)

Advanced control hardware for spin qubit experiments

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3. EeroQ Corporation, Chicago, United States,
4. QuTech and Kavli Institute of Nanoscience, Delft University of Technology, Delft, The Netherlands

Realizing a spin qubit universal quantum computer is an extremely complex task. To succeed, optimal control hardware is required, addressing the needs of spin qubit QPUs both at room temperature as well as cryogenic temperature. At room temperature, the seamless integration of OPX with QDAC-II offers an unparalleled solution for spin qubit QPU tune-up, enabling fast and advanced charge stability diagrams acquisition while retaining the best user experience. Furthermore, we show how the advanced capabilities of the OPX pulse processor can be harnessed to enhance the quality of qubit devices. This is achieved by the implementation of the on-the-fly Hamiltonian estimation protocols with real-time feedback on the qubit control sequence. At cryogenic temperatures, we introduce a new hermetically sealed packaging, enabling experiments in superfluid helium. A valuable way forward for large QPU could be operating processors in closed-loop liquid Helium systems, enabling the possibility to harness large cooling power as well as optimal QPU thermalization.

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