Se solute pinning and Kirkendall voiding of CdSeTe grain boundaries

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Se alloying of the CdTe absorber layer increases the short circuit current density by lowering the material band gap, while simultaneously maintaining the open circuit voltage through passivation and an enhanced carrier lifetime. In CdSe-CdTe devices Se alloying is achieved through inter-mixing of the two layers. If the starting CdSe layer is too thick Se over-alloying can occur, where a dramatic decrease in external quantum efficiency (EQE) is observed across a wide range of photon wavelengths. The microstructural origins of over-alloying has been investigated using a combination of cathodoluminescence (CL), electron backscattered diffraction (EBSD) and transmission electron microscopy (TEM) techniques. The Se inter-mixed region consists of small grains with a high density of porosity at the grain boundary triple points. Furthermore, we find evidence for faster Se diffusion along the grain boundaries. This has two important effects. First Se solute atoms at the grain boundary exert a pinning force that retards grain growth. The second is that a net vacancy flow is created due to the faster Se diffusion, which causes the grain boundary porosity (Kirkendall effect). The larger grain boundary area and free surfaces due to the pores lead to higher levels of non-radiative recombination and therefore a lower EQE. Our results uncover previously unreported deleterious effects of Se on the microstructure, that must be mitigated in order to achieve high efficiency devices.