

Development Status of the NOVA, COMET and STAR ASICs for Space Borne CCD Focal Plane Electronics

Matthew Clapp^{*a}, Nick Waltham^a, Quentin Morrissey^a, Chris Parmenter^a, Matthew Tildesley^a,
Stephen Bell^a, Lawrence Jones^a, Weihe Li^a

^aSTFC RAL Space, Rutherford Appleton Laboratory, Harwell Campus, Didcot, OX11 0QX

ABSTRACT

The increasing performance demands placed on spaceborne visible, near-IR and EUV focal plane instruments continue to drive the need for highly integrated, low noise, radiation tolerant readout electronics. In particular, modern science grade CCD systems require compact, low power solutions capable of supporting higher pixel rates, increasing numbers of detector outputs, and large multi-CCD focal plane assemblies, while maintaining stringent noise and reliability requirements. Application specific integrated circuits (ASICs) provide a practical route to achieving these objectives through functional integration and reduced dependence on discrete components.

This paper presents the current status of development of a new generation of mixed signal ASICs intended to form a complete chipset for CCD focal plane electronics: the NOVA video processing ASIC, and the high voltage COMET clock driver and STAR bias generation ASICs. Together, these devices are designed to address the full analogue interface between a CCD focal plane and downstream digital processing electronics.

The NOVA video ASIC is a dual channel CCD readout device providing low noise analogue amplification, optional on chip correlated double sampling, programmable gain and offset, and 16-bit analogue to digital conversion. The device has been designed to support both analogue and digital CDS modes, allowing optimisation across a wide range of pixel rates and noise requirements. The NOVA ASIC design has been completed and the die has been successfully fabricated. This paper summarises the design objectives, architectural features, and expected performance, and outlines the planned programme for packaging, laboratory characterisation, and radiation testing.

In parallel, two high voltage ASICs have been developed to provide the remaining CCD interface functions. The COMET ASIC is a six channel, high current clock driver offering fully programmable clock high and low voltage levels and controlled slew rate transitions, intended to drive both serial and parallel CCD clock phases. The STAR ASIC provides 24 independently programmable low noise DC bias outputs up to approximately 32 V, together with an integrated housekeeping telemetry system for monitoring internal and external voltages and temperatures. Both COMET and STAR have been fabricated, packaged, and subjected to initial laboratory based electrical testing.

Initial results are presented demonstrating correct functional operation, representative output waveforms, and measured performance consistent with design expectations for key parameters such as voltage range, drive capability, noise behaviour, and internal monitoring functionality. Finally, the paper summarises the current development status of the three ASICs and describes planned future work, including extended electrical characterisation, environmental testing, and radiation evaluation, aimed at enabling their use in future spaceborne CCD instruments.

Keywords: CCD focal plane electronics, ASIC, video processing, CCD clock drivers, high voltage bias generation, space instrumentation

1. INTRODUCTION

Scientific charge coupled devices (CCDs) continue to be widely used in space borne instrumentation for visible and extreme ultraviolet imaging applications, particularly where high quantum efficiency, excellent uniformity, and well understood radiation behaviour are required. While CMOS image sensors are increasingly adopted in some application areas, CCDs remain the preferred choice for many science missions. [1]

^{*} matthew.clapp@stfc.ac.uk; phone +44 1235 445906; <https://www.ralspace.stfc.ac.uk/>

The supporting focal plane electronics for CCD instruments present ongoing technical challenges. CCD operation requires multiple low noise DC bias voltages at elevated amplitudes, high current multi-phase clock waveforms with well controlled voltage levels and timing characteristics, and low noise video signal processing followed by high resolution analogue to digital conversion [2]. These functional requirements must be delivered within stringent constraints on mass, volume, power consumption, and long-term reliability, while also exhibiting tolerance to the space radiation environment.

Earlier generations of CCD controller electronics have relied extensively on discrete analogue and mixed signal components, resulting in relatively large and complex subsystems. Previous work by the authors demonstrated the benefits of replacing many of these functions with dedicated mixed signal application specific integrated circuits (ASICs), enabling significant reductions in system size, mass, and component count while improving functional integration and availability [3]. Subsequent work extended this approach through the development of dedicated high-voltage clock-driver and bias-generation ASICs intended for direct CCD interfacing [4][5].

Building on earlier CCD controller developments [6][7], a new generation of ASICs has been developed to further increase functional integration whilst reducing the size, mass and complexity of focal plane electronics.

This paper presents the current development status of three new ASICs intended to operate together to provide the core CCD focal plane electronics functionality:

- NOVA, a dual channel CCD video processing and digitisation ASIC;
- COMET, a programmable high current CCD clock driver ASIC;
- STAR, a high voltage CCD bias generation and telemetry ASIC [9].

The paper summarises the design objectives and architectural features of each device, presents initial laboratory-based test results for the COMET and STAR ASICs, and outlines planned future testing activities.

2. SYSTEM-LEVEL ARCHITECTURE

The NOVA, COMET and STAR ASICs are designed to operate together to provide a complete analogue interface between a CCD focal plane and downstream digital processing electronics. Figure 1 shows the intended system level architecture when used alongside a radiation tolerant FPGA providing timing generation, configuration control, and data handling.

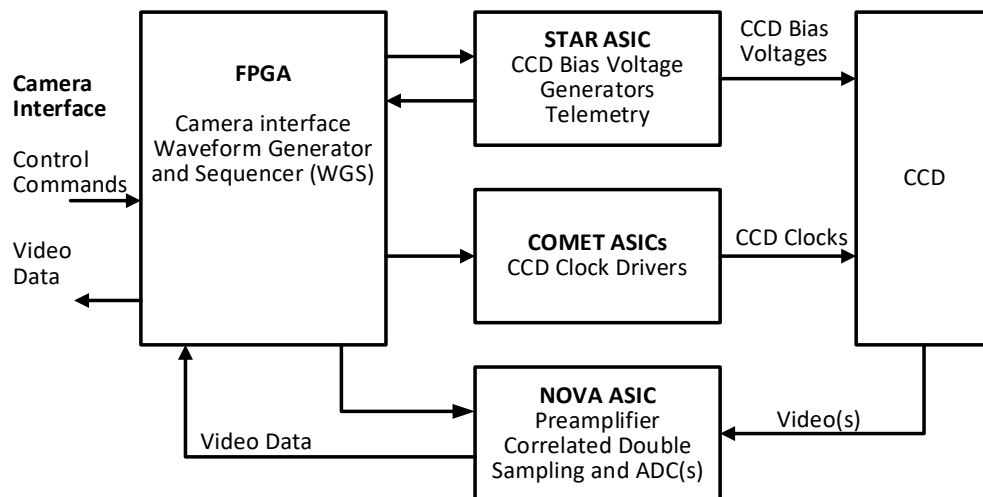


Figure 1. Intended system-level architecture of the NOVA, COMET and STAR ASIC chipset.

In this architecture:

- The COMET ASIC generates all CCD clock waveforms, providing programmable high and low voltage levels and controlled slew rate transitions with sufficient drive capability for both serial and parallel CCD registers.
- The STAR ASIC supplies all required CCD DC bias voltages and includes telemetry functions to monitor internal bias nodes, external voltages, and temperature sensors.
- The NOVA ASIC performs low noise analogue amplification, optional correlated double sampling (CDS), and analogue to digital conversion of the CCD video signals.

This functional partitioning simplifies board level design by separating low voltage analogue signal processing, high voltage bias generation, and high current clock driving into dedicated devices.

3. EVALUATION HARDWARE AND DEMONSTRATOR TESTING

3.1 Demonstrator Hardware

To support the validation of the high-voltage ASIC developments, a dedicated CCD controller demonstrator has been developed incorporating the COMET clock-driver and STAR bias-generation ASICs. The hardware is intended to provide a representative implementation of a CCD controller whilst also allowing detailed laboratory characterisation of the individual ASIC functions.

The demonstrator comprises a backplane and modular electronics architecture derived from previous CCD controller developments undertaken at STFC RAL Space. The system incorporates programmable CCD clock generation, CCD bias generation, telemetry monitoring and FPGA-based control functions. Dedicated evaluation circuitry has been included to facilitate measurement of ASIC supply currents, clock waveforms and bias-noise performance.

Photographs of the demonstrator hardware are shown in Figure 2. The COMET and STAR ASICs and associated support circuitry are shown on the right, closest to the backplane connector, while ASIC commanding is achieved via the FPGA shown in the bottom-left of the board.

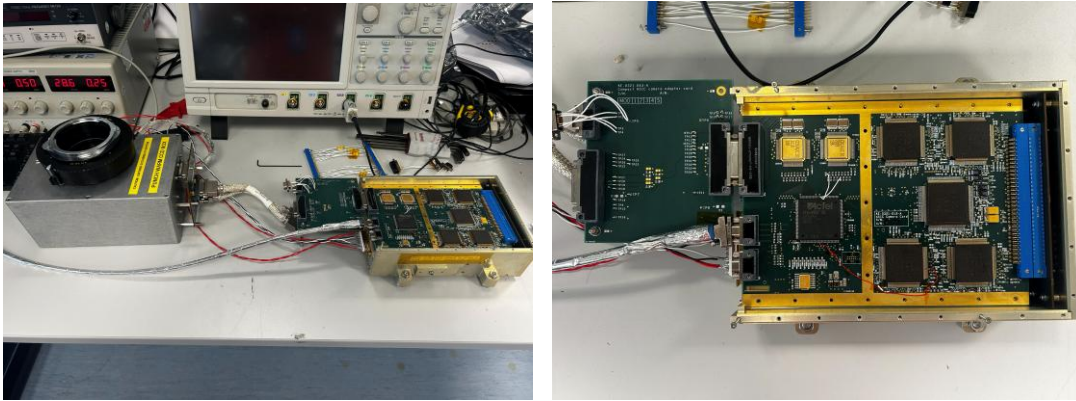


Figure 2. CCD controller demonstrator hardware incorporating the COMET and STAR ASICs.

3.2 Test Methodology

The demonstrator hardware has been used to perform initial functional and performance verification of the COMET and STAR ASICs. Measurements have focused on verifying correct operation of the programmable clock-driver and bias-generation functions together with obtaining representative performance data from the complete system.

The COMET output waveforms were characterised under representative loading conditions. Particular attention was given to evaluating clock amplitude, slew-rate control and phase overlap characteristics. Comparisons were also performed against equivalent clock waveforms obtained from a baseline CCD controller system to assess the performance of the

ASIC-based solution relative to a proven discrete design. A simplified schematic showing one image and serial clock phase of each configuration is shown in Figure 3 and Figure 4.

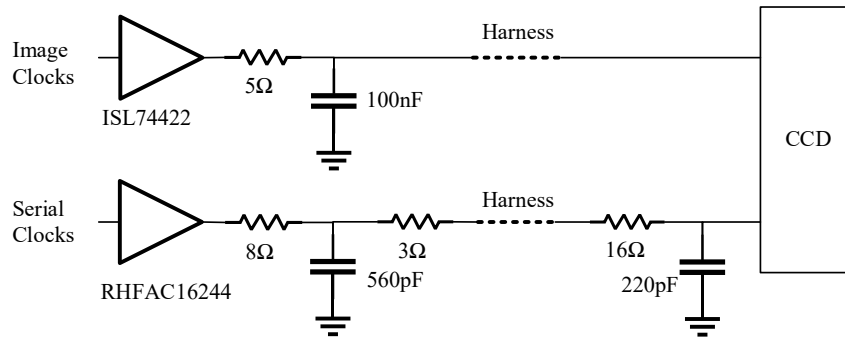


Figure 3. Simplified schematic of baseline CCD clock driver implementation used for baseline comparison with COMET ASIC implementation

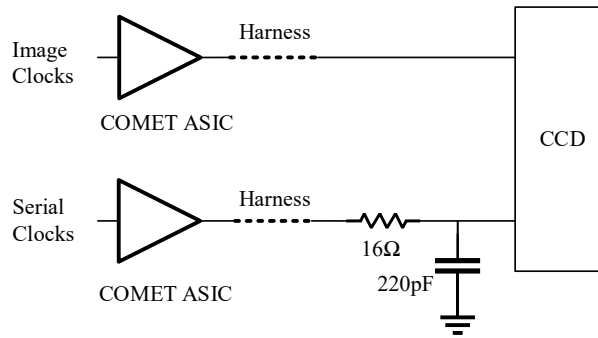


Figure 4. Simplified schematic of COMET ASIC CCD clock driver implementation

Bias-noise performance was investigated by routing the output-drain (OD) bias voltages directly to the video processing electronics and measuring the resulting increase in video-channel noise. This approach allows the noise contribution of the bias-generation circuitry to be estimated independently of normal CCD operation. Equivalent measurements were performed using both the STAR ASIC implementation and the baseline CCD controller hardware.

Current-consumption measurements were obtained using dedicated current-sense resistors incorporated into the demonstrator hardware. Measurements were performed in a range of operating modes, including standby, programmed, readout and CCD clear operation, allowing both ASIC-level and system-level power consumption to be assessed.

The results obtained using this hardware are presented in Sections 5 and 6.

4. NOVA CCD VIDEO PROCESSING ASIC

4.1 Design Objectives

NOVA has been developed as a next generation CCD video readout ASIC intended to support a wide range of CCD operating modes and pixel rates while maintaining low noise performance. Key design objectives include:

- two independent CCD video channels per device;
- low input referred noise suitable for scientific imaging;
- optional on chip analogue CDS;
- support for digital CDS at lower pixel rates [8];
- high resolution analogue to digital conversion;
- low power standby modes during CCD integration periods.

4.2 Architecture Overview

Each NOVA ASIC integrates two identical video channels. Each channel includes a pseudo differential input stage with DC restoration circuitry, allowing CCD outputs to be AC coupled and removing large DC offsets at the CCD output node. The input stage feeds a programmable preamplifier and gain stage with adjustable offset capability.

Two operational modes are supported. In analogue CDS mode, on chip sampling circuitry performs correlated double sampling synchronised to the CCD timing, producing a single output sample per pixel. In digital CDS mode, the analogue front end operates continuously and the ADC is clocked at a higher rate, allowing multiple samples of the reset and signal levels to be digitised for subsequent off-chip processing.

Analogue to digital conversion is performed using a 16-bit pipeline architecture, designed to provide sufficient resolution, linearity, and bandwidth for anticipated CCD applications. Configuration and control are provided through a serial digital interface, and data are transmitted via LVDS outputs to minimise digital noise coupling.

Key characteristics of the NOVA ASIC are presented in Table 1. The values presented represent architectural design targets and expected operating characteristics derived from simulation and design analysis. Electrical characterisation of packaged devices is planned following completion of package assembly.

Table 1. NOVA ASIC key characteristics

Parameter	Value
CCD channels	2
ADC resolution	16-bit
Maximum ADC rate	12 MSPS
Maximum pixel rate	6 Mpixels/s
Input referred noise (target) (ACDS, 2 Mpixels/s, 1 V input range)	17 μ V rms
CDS modes	Analogue and Digital
Output interface	LVDS DDR
Supply voltage	3.3 V
Typical power	~430 mW
Operating temperature range	-50 °C to +125 °C
Current status	Fabricated, awaiting test

4.3 Fabrication status

The NOVA ASIC design has been completed and the die has been successfully fabricated in a radiation tolerant CMOS process. At the time of writing, the device has not yet been packaged and no electrical characterisation has been performed.

4.4 Planned Verification Activities

Following packaging, NOVA will be subjected to a structured verification programme including:

- basic functional testing and interface validation;
- analogue performance characterisation (noise, linearity, bandwidth);
- power consumption measurements in different operating modes;
- temperature dependent testing across the intended operating range;
- radiation testing to characterise total ionising dose and single event behaviour.

5. COMET HIGH CURRENT CCD CLOCK DRIVER ASIC

5.1 Design Overview

COMET is a six-channel CCD clock driver ASIC designed to generate multi-level clock waveforms with programmable voltage levels and controlled transition rates. A detailed description of the architecture and initial device characterisation has been reported previously [5].

Clock output voltage levels are programmable over a range of approximately 0 V to 16 V, while the driver current settings determine clock rise and fall times.

5.2 Fabrication and Packaging

The COMET ASIC has been fabricated and packaged in a ceramic package suitable for laboratory evaluation.

5.3 Initial Laboratory Results

Initial laboratory testing has been performed using the demonstrator hardware described in Section 3 to verify correct functional operation and characterise representative clock-waveform behaviour.

Particular attention was given to the generation of serial clock waveforms and the effect of programmable driver current settings on clock shape. Figure 5 shows representative serial clock waveforms obtained before and after adjustment of the output drive current. The initial settings produced observable overshoot on several clock phases. By reducing the programmed drive current the overshoot was substantially reduced whilst maintaining the required clock amplitude and phase overlap. The results demonstrate that the programmable output stage can be used to optimise clock waveform quality for a particular CCD load.

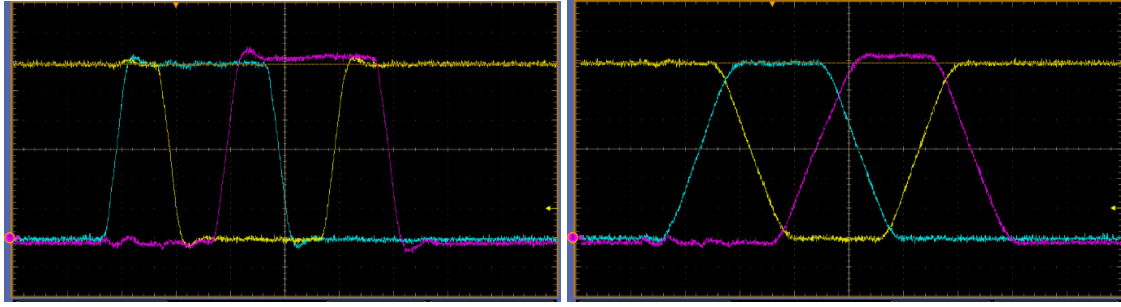


Figure 5. Representative serial clock waveforms obtained before (left) and after (right) adjustment of the output drive current registers. All traces are 1 V/div shown with a 100 ns/div time-base.

Initial serial clock measurements exhibited transient effects on neighbouring clock phases during switching events. The magnitude of these features were reduced through optimisation of the programmable output drive settings, as shown in Figure 5. Some residual coupling between adjacent phases remained visible and is believed to be influenced by the inter-phase capacitance of the CCD load. Large-area CCD clock structures exhibit significant capacitive coupling between adjacent phases. Consequently, transitions on one phase are expected to induce transient responses on neighbouring phases, particularly when operating with fast clock edges. [2]

Additional measurements were performed on the image clock outputs using a range of programmed driver current settings. Figure 6 shows representative image clock waveforms obtained using low and high programmed driver current settings. As expected, increasing the programmed drive current reduced rise and fall times, whilst lower drive settings produced slower transitions. Stable operation was observed over the complete range of settings tested.

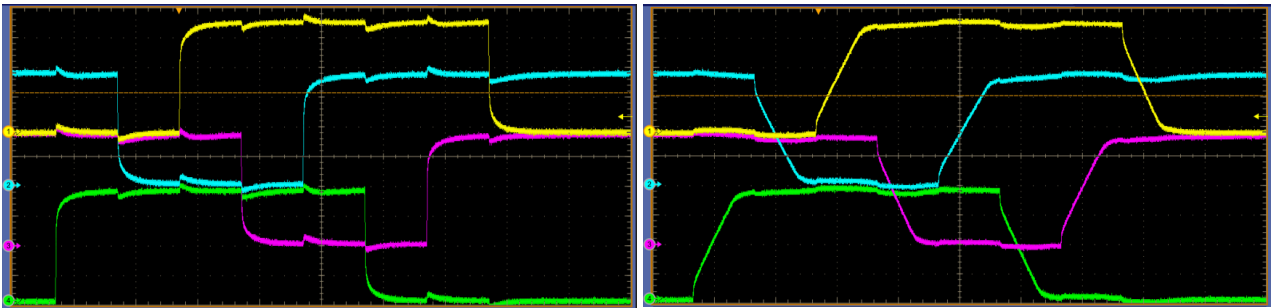


Figure 6. Representative image clock waveforms obtained using a range of programmed driver current settings. The left image shows the waveforms at a near maximum driver current setting (0x380); the right image shows the waveforms at a near minimum setting (0x080). All traces are 2 V/div shown with a 10 µs/div time-base.

To quantify the effect of the programmable output-current setting, rise and fall times were measured for a representative serial clock output over a range of current drive settings. The results are shown in Figure 7. Increasing the current drive setting reduced the measured edge time from approximately 167 ns at a setting of 0x03F to approximately 20 ns at the maximum setting of 0x3FF. These results demonstrate the wide range of edge-rate control available within the COMET architecture allowing clock waveform characteristics to be optimised for differing CCD load conditions.

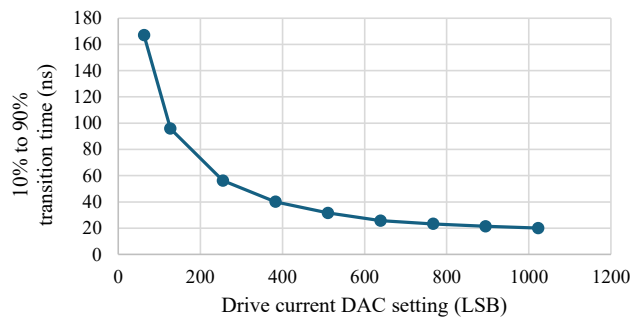


Figure 7. Measured serial-clock rise and fall times as a function of COMET drive current setting.

A comparison was also performed between the COMET-generated clock waveforms and equivalent waveforms produced by the baseline CCD controller implementation. Representative serial and image clock waveforms are shown in Figure 8 and Figure 9. The measured waveforms demonstrate comparable clock amplitudes and overlap behaviour and are consistent with those required for operation of science-grade CCD detectors.

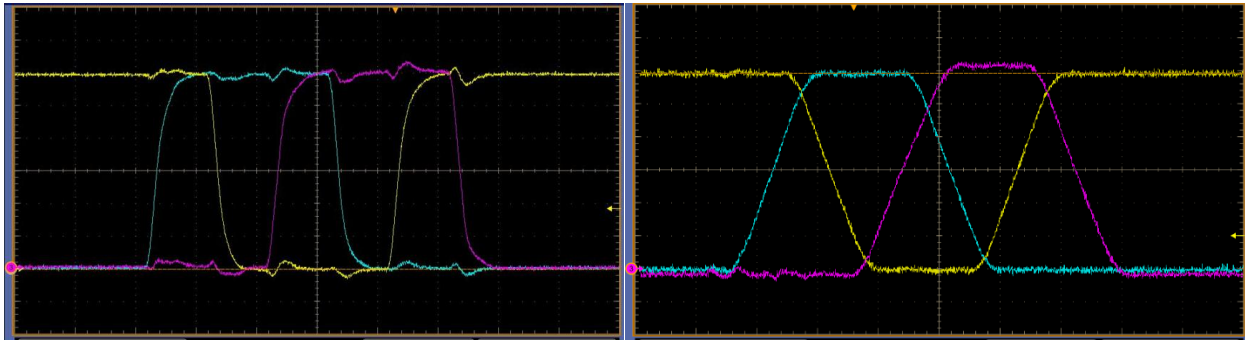


Figure 8. Representative serial clock waveforms obtained using a baseline CCD clock driver implementation (left) and the equivalent using the COMET ASIC (right). All traces are 1 V/div shown with a 100 ns/div time-base.

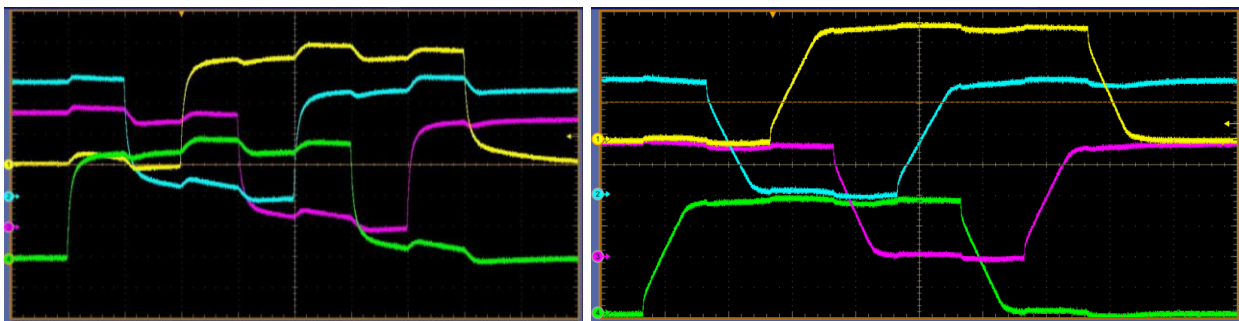


Figure 9. Representative image clock waveforms obtained using a baseline CCD clock driver implementation (left) and the equivalent using the COMET ASIC (right). All traces are 2 V/div shown with a 10 μ s/div time-base.

Supply current measurements were obtained using current sense resistors incorporated on the ASIC evaluation hardware. For the image-clock COMET device, the 15 V supply current increased from approximately 5 mA in the unprogrammed state to approximately 9.5 mA following programming, with peak currents of up to 35 mA observed during CCD readout operations. For the serial-clock COMET device, peak 15 V current consumption of approximately 30 mA was measured during readout. These results were found to be broadly consistent with pre-existing characterisation data obtained during device development [5].

6. STAR HIGH VOLTAGE CCD BIAS AND TELEMETRY ASIC

6.1 Design Overview

The STAR ASIC provides 24 independently programmable DC bias outputs for CCD operation, each capable of delivering voltages up to approximately 32 V. Each output includes current limiting and is designed for stable operation with capacitive loads.

In addition to bias generation, STAR integrates a telemetry subsystem allowing measurement of internally generated bias voltages, application specific external voltages, and differential temperature sensor inputs all via an on-chip ADC.

A detailed description of the architecture and initial die-level characterisation has been reported previously [9].

6.2 Fabrication and Packaging

The STAR ASIC has been fabricated and packaged using a ceramic package similar to COMET.

6.3 Initial Laboratory Results

Initial laboratory testing has been performed using the demonstrator hardware described in Section 3 to verify operation of the STAR bias generation and telemetry ASIC. Correct generation of the programmed CCD bias voltages was observed across the full operating range of the device and successful operation of the telemetry subsystem was demonstrated through measurement of internal and external housekeeping signals.

The accuracy of the telemetry subsystem was assessed by comparing ADC-derived measurements against independently measured supply voltages on the demonstrator hardware. Representative results showed agreement typically within approximately 1% of the reference measurements across the monitored voltage range. These tests confirmed correct operation of the telemetry signal path, including the analogue multiplexer, programmable gain stage and ADC.

A series of measurements was performed to evaluate the contribution of the STAR output drain (OD) bias circuitry to the overall video noise performance. The test method involved routing the OD bias directly to the video processing inputs whilst grounding the opposing input, thereby allowing the bias noise contribution to be estimated independently of normal CCD operation.

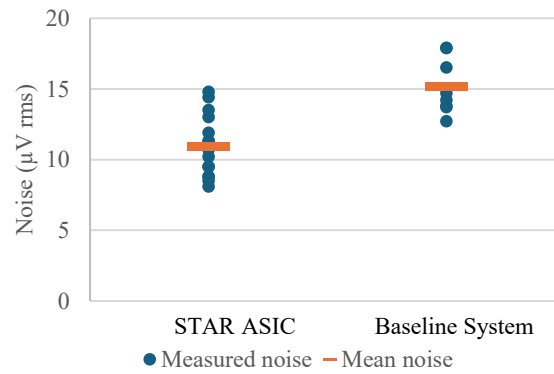


Figure 10. Estimated output-drain (OD) noise contribution for the STAR ASIC and a representative baseline CCD controller implementation. Individual measurements are shown together with the mean value for each test system.

The measured baseline noise with both video inputs grounded was typically 2.7 ADU rms. When the STAR OD outputs were connected to the video processing chain, only a modest increase in measured noise was observed. Analysis of the resulting data indicates an output-drain noise contribution typically between approximately 8 μV rms and 15 μV rms depending on configuration and measurement channel.

Equivalent measurements were subsequently performed using a baseline CCD controller implementation for comparison. The corresponding measured output-drain noise contributions were generally within the range of approximately 13 μV rms to 18 μV rms. Although additional testing is required to establish full statistical confidence, the results indicate that the STAR-generated bias outputs provide noise performance comparable with the existing implementation and, in several measurement configurations, exhibited a lower estimated OD noise contribution.

The influence of additional output decoupling was also investigated. A 3.3 μF capacitor together with a 10 nF ceramic capacitor was connected between the OD output and ground. Following the addition of local decoupling, a further reduction in the measured noise contribution was observed, with measured values approaching the baseline noise floor of the video processing electronics. This result suggests that local output capacitance may provide a simple method of further reducing bias noise where required by the application.

Supply current measurements were also performed. The STAR ASIC consumed approximately 5 mA from the 30 V rail in the unprogrammed state and approximately 28 mA to 33 mA immediately following bias programming. During normal readout operation the measured 30 V rail current was approximately 32 mA. The corresponding 3.3 V supply current was approximately 17 mA following configuration.

These measurements demonstrate that the STAR ASIC can provide both CCD bias generation and housekeeping telemetry functionality whilst maintaining output noise performance comparable to an established flight-derived CCD controller architecture.

7. INTEGRATED CHIPSET PERSPECTIVE

When combined, the NOVA, COMET, and STAR ASICs form a highly integrated solution for CCD focal plane electronics. Compared with traditional discrete implementations, this approach offers:

- significant reduction in PCB area and component count;
- simplified power distribution and bias generation;
- improved configurability and flexibility;
- clear scalability to multi-CCD focal planes.

A single FPGA can configure and coordinate all three devices, further simplifying the system level design.

The demonstrator hardware has shown that the COMET and STAR ASICs can successfully replace substantial portions of the discrete analogue circuitry traditionally required to generate CCD clock waveforms and bias supplies. Together with the NOVA ASIC, the resulting chipset has the potential to provide a highly integrated controller solution suitable for future multi-output CCD and large focal-plane applications, where increasing levels of functional integration become necessary to control system size, mass and power consumption. [3]

8. FUTURE WORK AND CONCLUSION

This paper has presented the development status of the NOVA video processing ASIC and initial laboratory results from the COMET clock driver and STAR bias generation ASICs. NOVA has completed design and fabrication and is awaiting packaging and test. COMET and STAR have been packaged and demonstrated correct functional behaviour under initial laboratory testing.

Future work will focus on extended characterisation, environmental testing, and radiation evaluation of all three devices, with the aim of enabling their use in future space borne CCD instruments.

ACKNOWLEDGEMENTS

The authors would like to acknowledge Mark Prydderch who contributed to the design of STAR and COMET, and Martin Torbet and Jack Stapleton who both contributed to the testing and verification of these devices.

Generative artificial intelligence tools were used to assist with drafting and refinement of the manuscript text. All technical content, analyses, results and conclusions were reviewed and validated by the authors, who accept full responsibility for the contents of the paper.

REFERENCES

- [1] Waltham, N.R., "CCD and CMOS Sensors", in *Observing Photons in Space*, Springer (2013).
- [2] Janesick, J., *Scientific Charge-Coupled Devices*, SPIE Press (2001).
- [3] Waltham, N., Morrissey, Q., Clapp, M., Bell, S., Jones, L., and Torbet, M., "The design and development of low- and high-voltage ASICs for space-borne CCD cameras," *CEAS Space Journal* 9, 531-544 (2017). DOI: 10.1007/s12567-017-0181-5.
- [4] Morrissey, Q., Bell, S., Jones, L., Prydderch, M., Torbet, M., Waltham, N., and Clapp, M., "A pair of custom ASICs for bias generation and clock buffering in space-based CCD camera systems," *Proc. SPIE 10709, High Energy, Optical, and Infrared Detectors for Astronomy VIII*, 107092T (2018). DOI: 10.1117/12.2312623.

- [5] Morrissey, Q., Bell, S., Jones, L., Torbet, M., Waltham, N., and Clapp, M., "A multi-channel CCD clock driver ASIC for space-based applications," IEEE Nuclear Science Symposium, Medical Imaging Conference and Room-Temperature Semiconductor Detector Workshop (NSS/MIC/RTSD), Strasbourg, France (2016).
- [6] Waltham, N. R. and Eyles, C. J., "Design, development and performance of the STEREO SECCHI CCD cameras," Proc. SPIE 6689, Solar Physics and Space Weather Instrumentation II, 668908 (2007). DOI: 10.1117/12.733835.
- [7] Waltham, N. R., Beardsley, S., Clapp, M., Lang, J., Jerram, P., Pool, P., Auken, G., Morris, D., and Duncan, D., "Systems approach to the design of the CCD sensors and camera electronics for the AIA and HMI instruments on Solar Dynamics Observatory," Proc. International Conference on Space Optics (ICSO 2010), Rhodes, Greece (2010).
- [8] Clapp, M. J., "Development of a test system for the characterisation of DCDS CCD readout techniques," Proc. SPIE 8453, 84531D (2012).
- [9] Morrissey, Q., Waltham, N., Bell, S., Prydderch, M., Torbet, M., and Clapp, M., "A complete space based CCD biasing solution in a 0.35 μm high voltage CMOS ASIC," Proc. 5th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications (AMICSA 2014), pp. 59-64 (2014).