Low Latency On-Board Data Handling for Earth Observation Satellites using Off-the-Shelf Components

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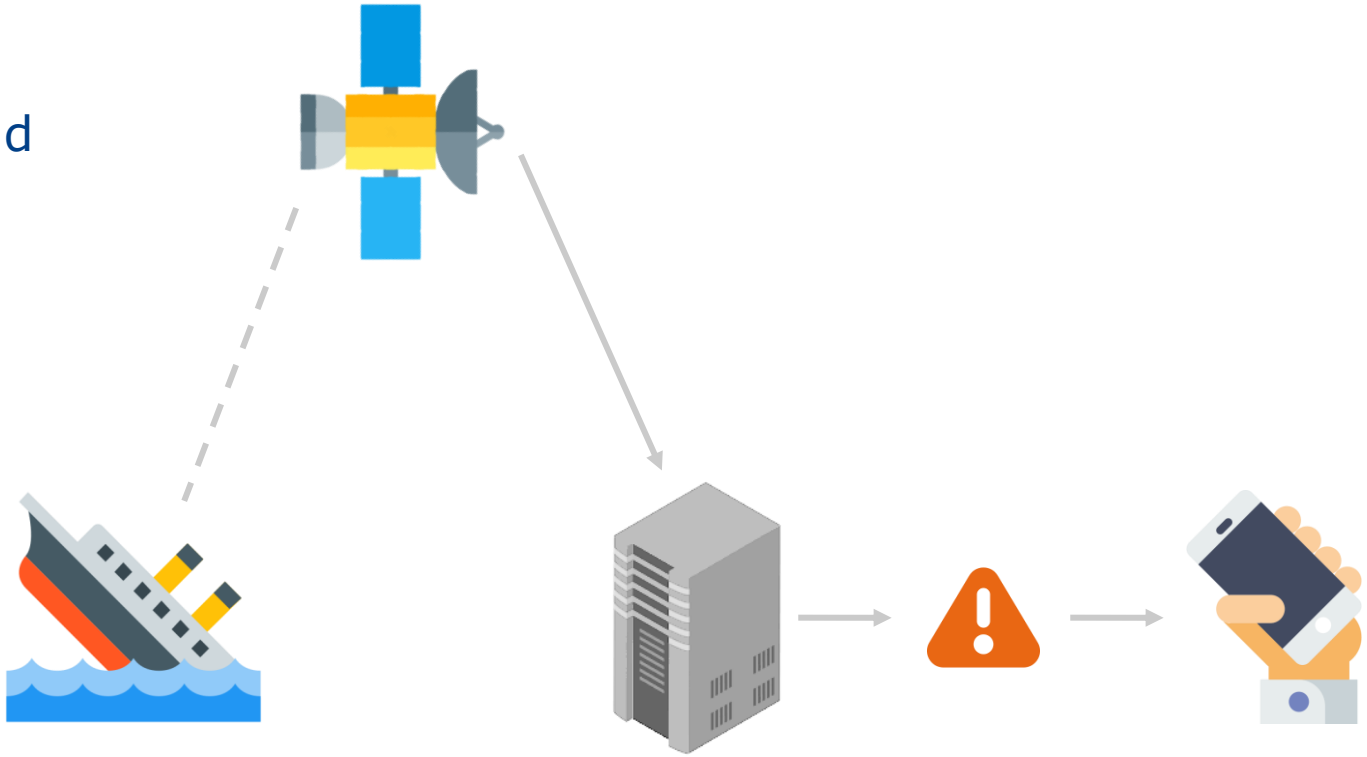
INTRODUCTION

Motivations

Traditional satellite **Earth Observation** system:

- Acquired image data compressed and transmitted to ground
- Image processing performed at ground



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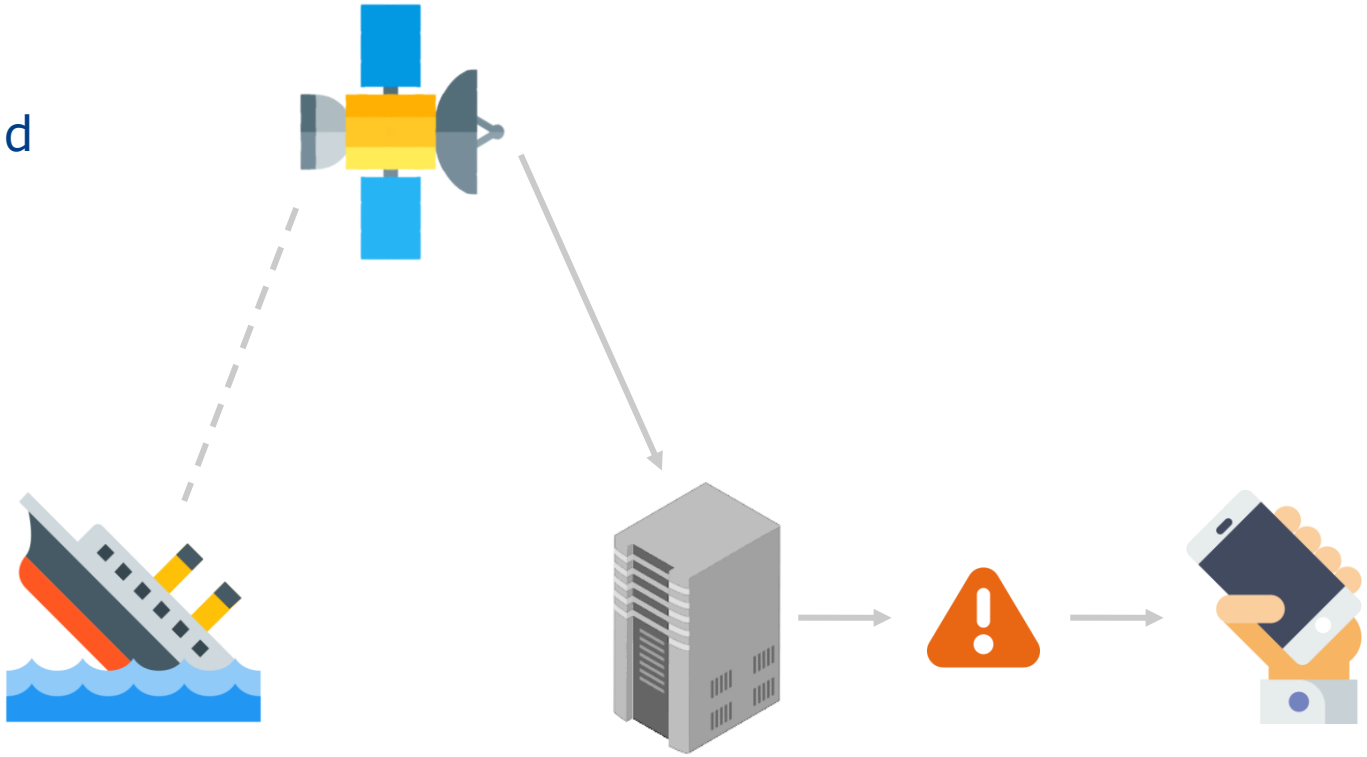
Data **transmission** is a
bottleneck for latency



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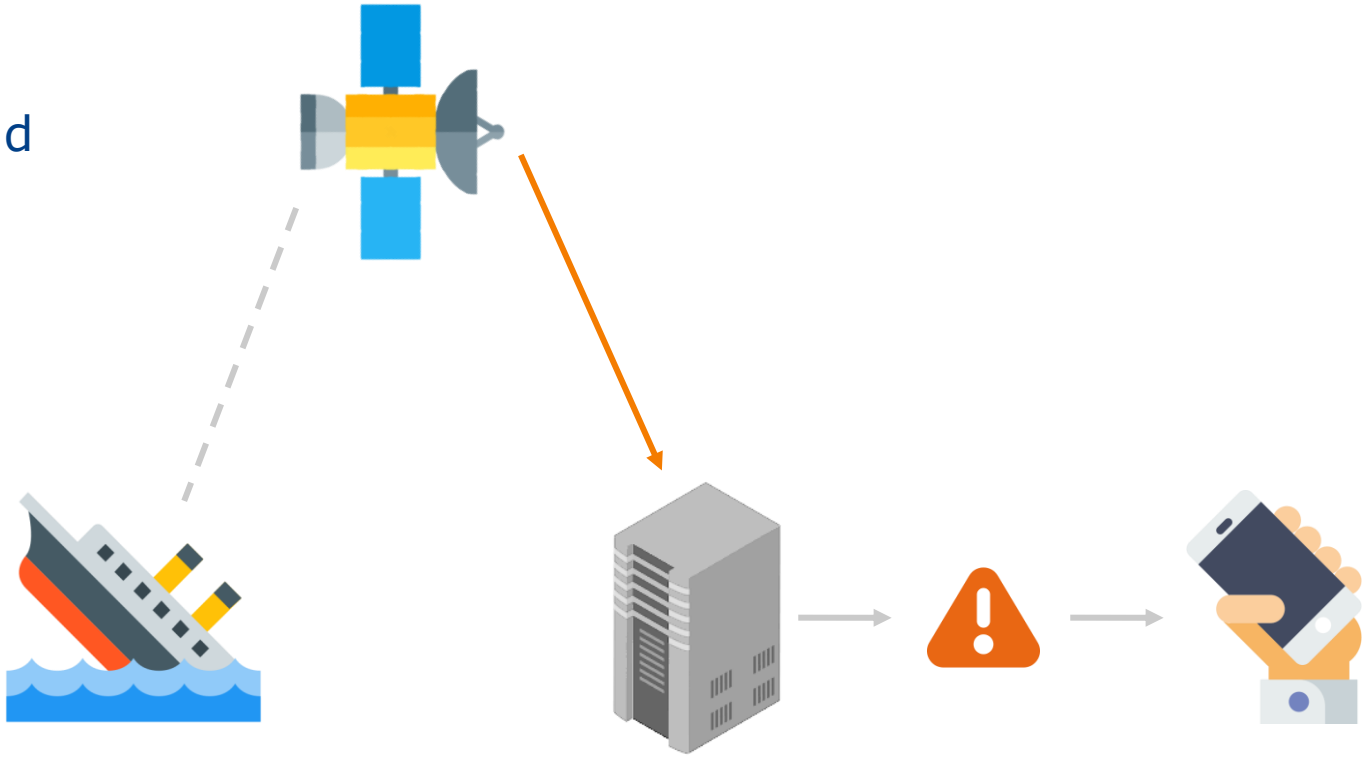
Near Real-Time alert delivery to the end user:

1h - 3h



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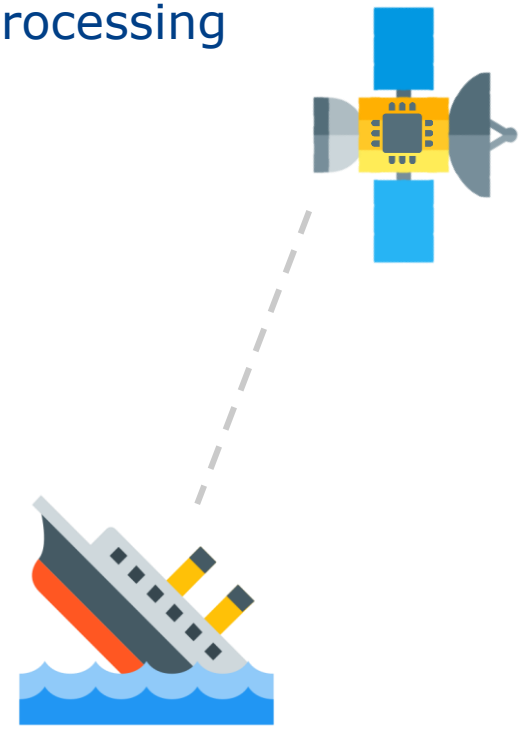
EO-ALERT system:

- Also perform image generation and processing **on-board**



Motivations

EO-ALERT system:

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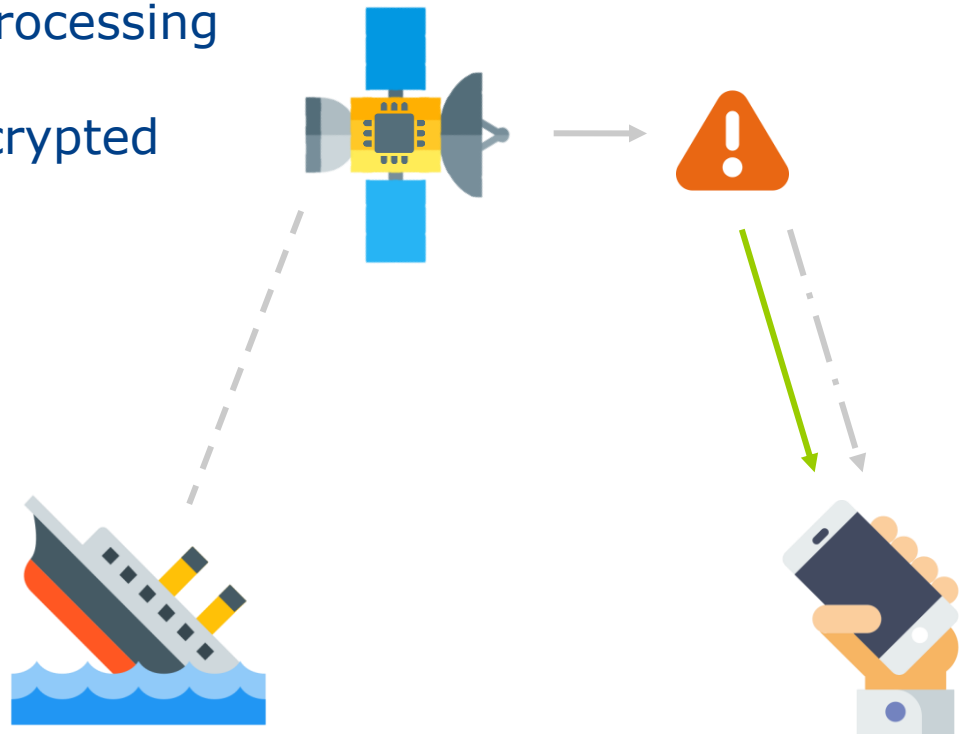
- Only transmit compressed and/or encrypted data when needed



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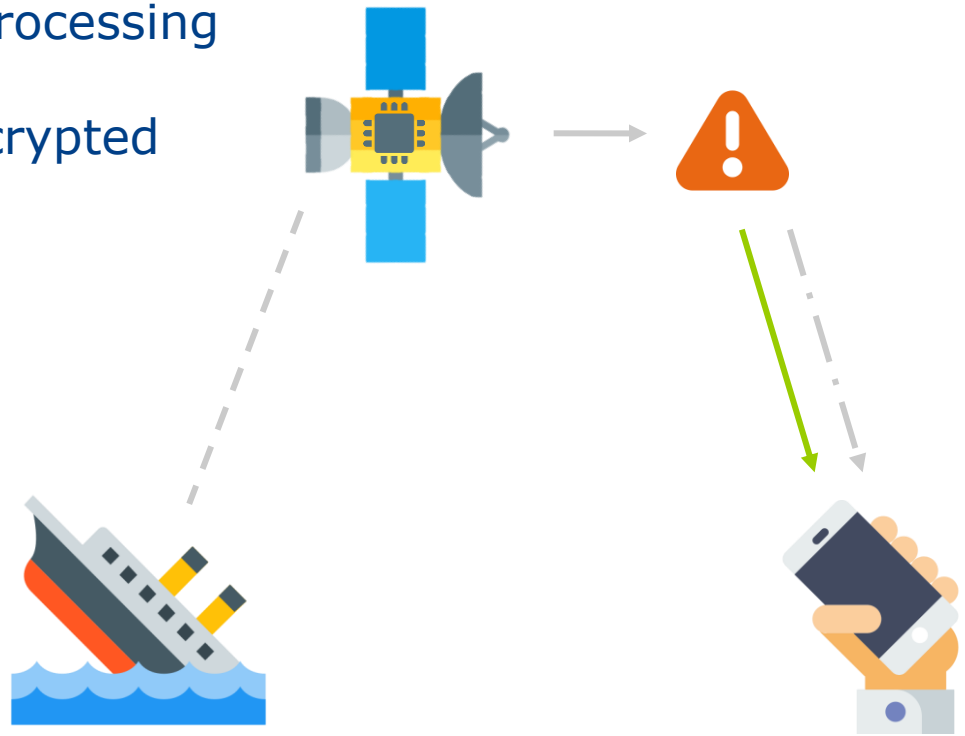
True Real-Time alert delivery to the end user

< 5 min



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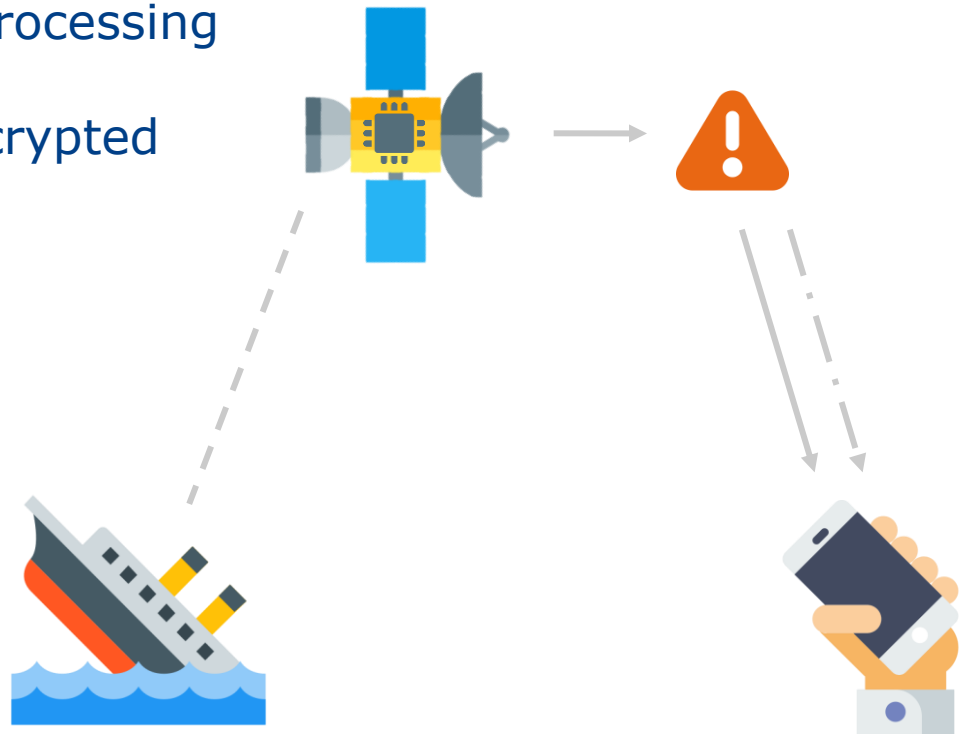
Compression & Encryption are now **critical** for latency



IMPLEMENTATION

Implementation

- **Reconfigurable** and **modular** data handling subsystem

- **Latency-optimized** compression and encryption subsystem

Implementation

- **Reconfigurable** and **modular** data handling subsystem
- **Latency-optimized** compression and encryption subsystem

- **High-performance commercial MPSoC** (µP + FPGA)
  - **Multithreaded SW** for data handling and general-purpose compression-encryption
  - Image compression **hardware accelerator**

Image Compression Accelerator

Desired features:

- CCSDS-123.0-B-2 recommended standard + encryption
- Support for **single- and multi-band optical or SAR** raw data and generated images with arbitrary dimensions and dynamic range
- Support for **runtime parameter tuning**:
  - **Lossless** or **near-lossless** compression
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Time consuming

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Use state-of-the-art **High-Level Synthesis** EDA tools

Use existing C code

Effortless validation

Maintain SW features

HLS Design and Verification Methodology

1) Define and develop a **test suite** to monitor the performance of the of the hardware-oriented model compared to the original one

2) Establish a subset of the above test suite to **verify the correctness** of the synthesised RTL

3) Rework the reference C code to implement the desired features (hardware-oriented code)

4) Further modify the model to **suit the target HW platform**

5) Evaluate the run-time hardware performance of the new model with 1) and 2) and iterate 4)

6) Wrap the hardware implementation in an **IP core** to be instantiated on the target platform

7) Develop **software APIs to access the IP core** from the software running on the μP

8) Validate the instantiated IP core and assess its **performance**

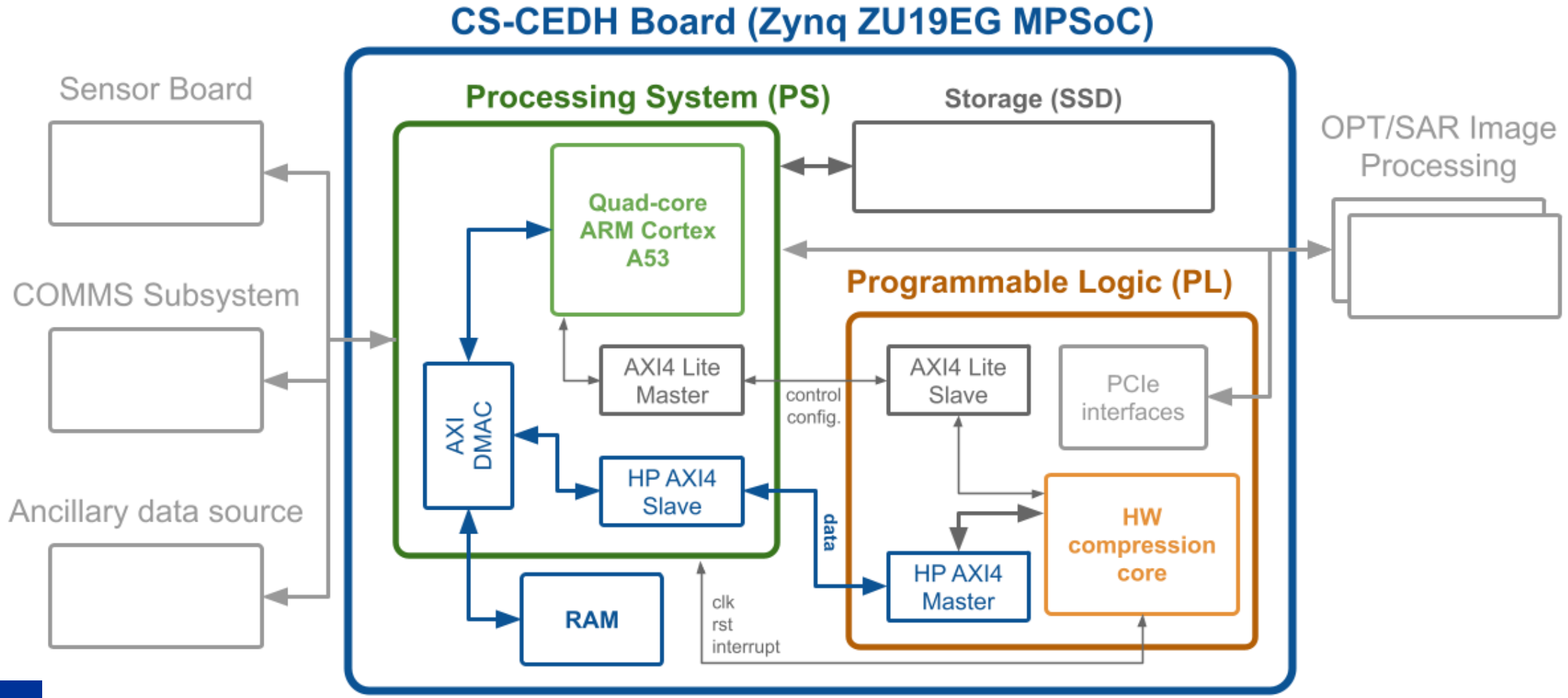
Target HW Platform

Commercial-grade **Xilinx Zynq™ UltraScale+™ ZU19EG MPSoC** on ProFPGA Uno motherboard

- Processing System (PS):
  - Quad-core ARM® Cortex™-A53
  - Dual-core ARM® Cortex™-R5
  - 4GB DDR4 ECC memory
- Programmable Logic (PL):
  - 1M CLB flip-flops
  - 522k CLB LUTs
  - 984 block RAM tiles (4.3MB)
  - 5x PCIe Gen3 x16
  - 1,968 DSP slices
- Connectivity and storage expansion boards

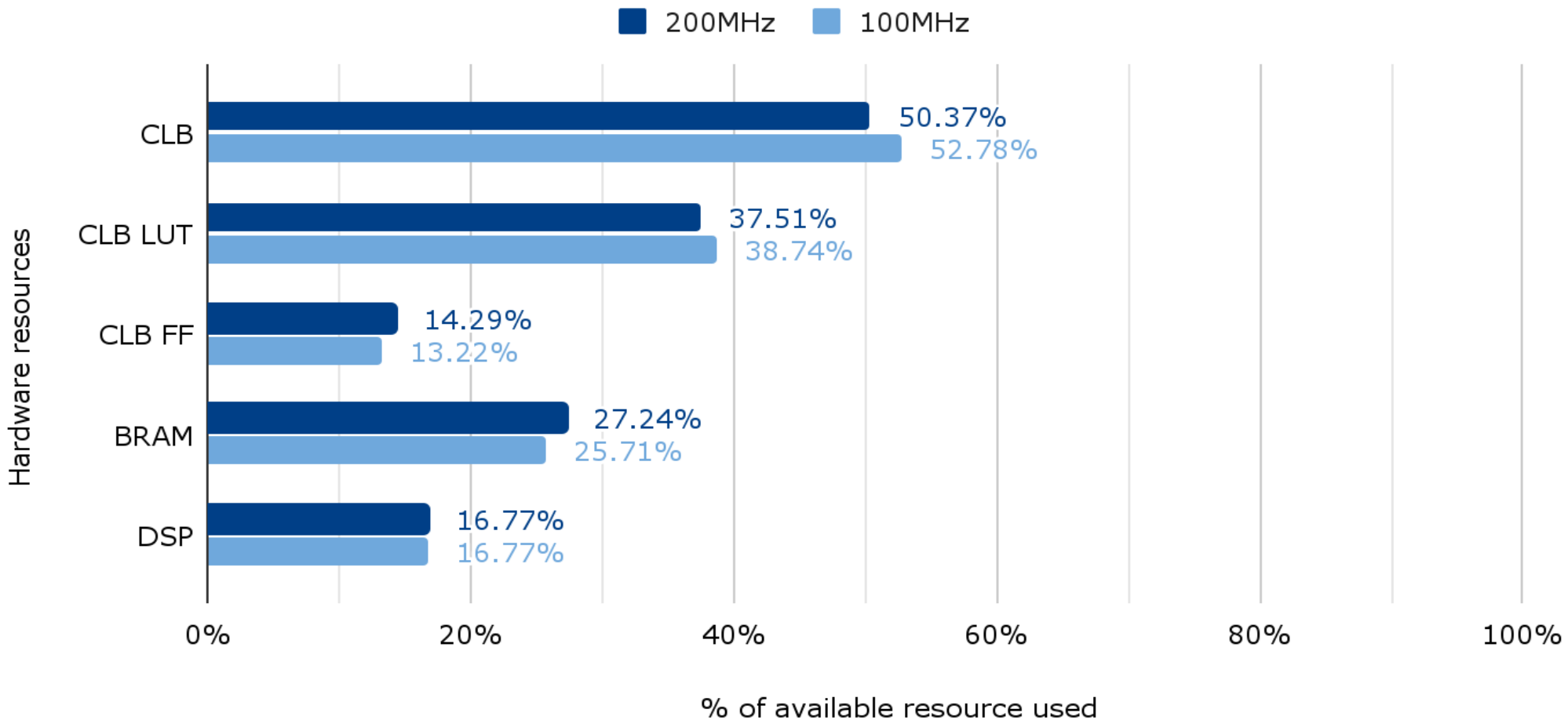
© Mentor Graphics https://www.xilinx.com/products/boards-and-kits/1-rv9gr8.html

System-Level architecture

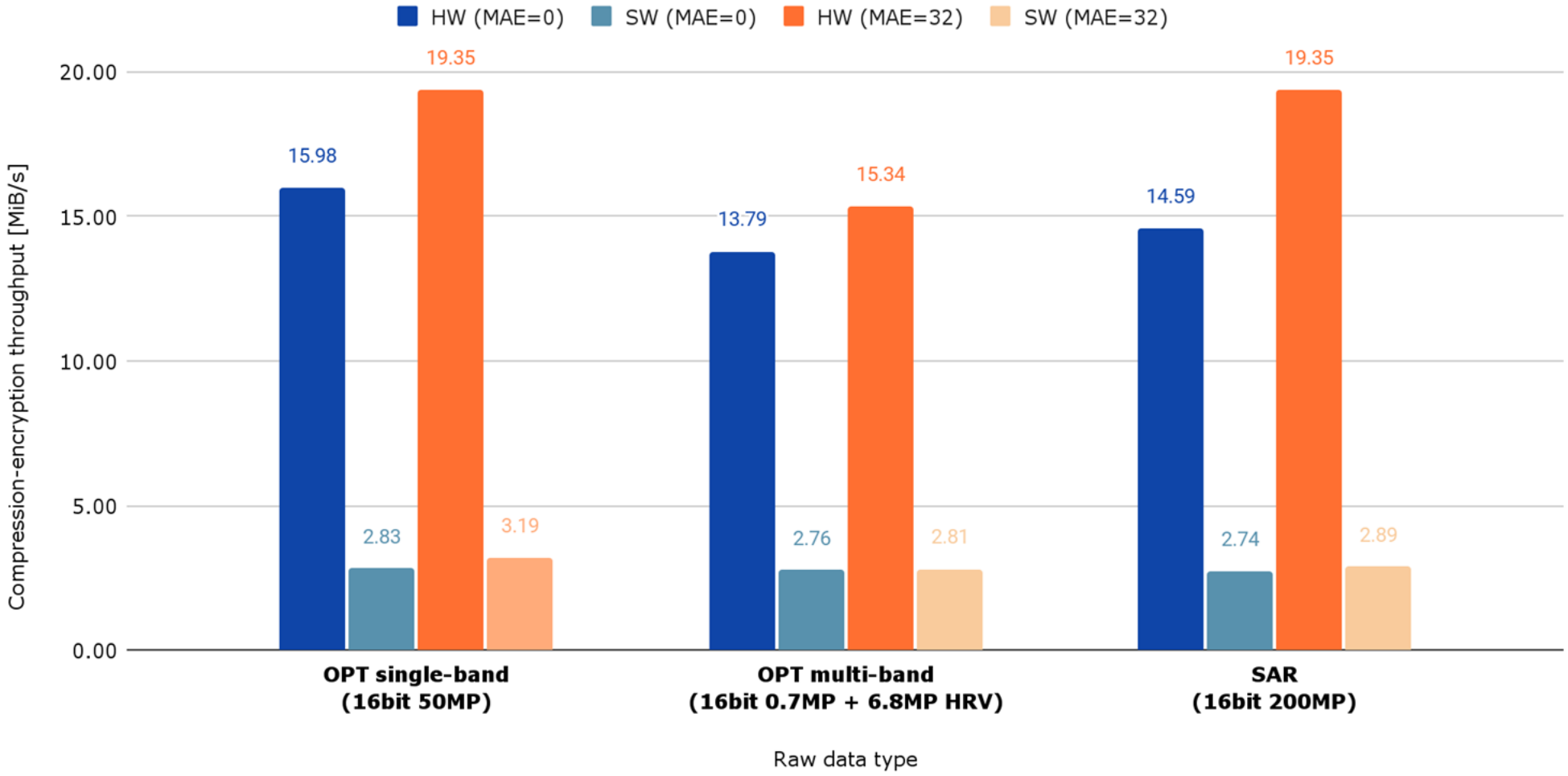


RESULTS

Resource Usage



HW vs. SW Performance



Contribution to overall system latency

- **10x 50MP optical raw data + 3x 50MP generated images + 26x 10kB alerts**
  - With SW C/E: 1300s
  - With HW C/E: 310s

~4x faster

- **10x (0.7MP 5-band + 6.8MP single-band) optical raw data + 10x (0.7MP 5-band + 6.8MP single-band) generated images + 4x 20kB alerts**
  - With SW C/E: 170s
  - With HW C/E: 70s

~2.5x faster

- **3x 200MP SAR raw data + 3x 30MP generated images + 13x 10kB alerts**
  - With SW C/E: 960s
  - With HW C/E: 225s

~4x faster

Future Perspectives

- Multiple (smaller) compression/encryption hw accelerators on the same FPGA
- Encryption-only hardware accelerator (stream cypher)
- Direct interface between compression/encryption accelerator and PCIe
- Use the R5 core instead of the A53 core to save power and better support hard real-time data handling tasks (e.g., alert encryption and transmission)

The End

Thank you for your attention