

Control and improvement of wafer bow in dual ion beam deposited thin-film optical stacks for enhanced SNSPD performance

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ABSTRACT

Superconducting nanowire single-photon detectors (SNSPDs) are the most advanced and reliable technologies for detecting single photons. A key challenge in improving detection efficiency lies in maximizing the optical absorption within the superconducting nanowire. One strategy is to integrate highly reflective mirrors such as Distributed Bragg Reflectors (DBRs) beneath the nanowire layer to enhance the optical field intensity at detector surface. However, previous implementations have been hindered by the surface roughness of conventional DBR deposition techniques, which are incompatible with the smoothness requirements of SNSPD. Low surface and interface roughness minimizes optical scattering losses, thereby preserving the high reflectivity of the multilayer mirror, while simultaneously providing a homogeneous surface for the deposition of ultrathin superconducting films, where even small thickness variations may influence current uniformity and device performance. A target roughness in the order of 0.1 nm was therefore pursued. Dual ion beam sputtering (DIBS) offers a promising solution for fabricating dense, low-defect optical multilayer stacks with low surface roughness, which serve as DBRs with high reflectivity in different wavelength regimes. In this work, we investigate the deposition of DBR mirrors on 4-inch silicon wafers using DIBS to ensure optimal optical and mechanical properties. A major challenge of this deposition technique is the intrinsic film stress, leading to significant wafer bowing which complicates subsequent lithographic steps and can exceed the depth of focus limits of electron-beam lithography systems. We systematically investigate several approaches to controlling and minimizing wafer bow in DIBS-deposited Ta₂O₅/SiO₂ DBR and compare experimental results with corresponding simulations.

Keywords: SNSPD, DBR, Ta₂O₅/SiO₂, DIBS, wafer bow reduction

1. INTRODUCTION

The use of encryption is becoming increasingly important for secure data transmission. One option for this is the quantum key distribution (QKD). This process involves the exchange of a secret cryptographic key between two parties, while allowing the detection of any eavesdropper attempts. The code of the key consists of individual photons that are transmitted as the encrypted medium [1]. Superconducting nanowire single photon detectors (SNSPD) are one of the technologies employed at the receiver for single photon detection [2]. In its ground state, the superconducting nanowire is a current-carrying superconductor. When the wire absorbs a photon, it generates a resistance (hotspot). The hotspot forms a vortex-antivortex pair that spreads across the cross-section of the nanowire, heating the nanowire and thereby suppressing the superconducting state. The measured voltage signal rises due to the generated resistance. Once the hotspot has spread across the cross-section, it continues to propagate along the length of the nanowire due to Joule heating. The measured signal has now reached its peak and subsequently flattens out again as the wire returns to its ground state [2] [3].

2. SNSPD PERFORMANCE ASPECTS

An important performance factor is the number of registered signals per second, i.e. false counts where no photon is detected. This is referred to as the dark count rate (DCR). The DCR is much lower for SNSPD than for single photon

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avalanche diodes (SPAD): 1–100 cps compared to 100–10⁶ cps [4][5]. Low DCRs play an important role in low-earth orbit (LEO)-ground quantum key distribution (QKD) [6] and deep-space optical communication [7], as these applications benefit from very low count rates.

Another important parameter for SNSPDs is the timing jitter. This describes the uncertainty in the arrival time of a photon and is more precisely defined as the time difference between the photon being captured and the electrical pulse being registered. The comparison of SPADs with SNSPD here shows a clear difference. For SPADs, this value lies between 20 and 180 ps [8]. In contrast, the electrical pulse in SNSPD is detected after just < 3–20 ps [9]. A lower value is particularly advantageous in applications such as Light Detection and Ranging (LiDAR) [10], time-of-flight [10], and quantum communication [9].

In photon transmission, the probability of an incident photon being detected is described by the system detection efficiency (SDE). For a nanowire on a substrate, this typically ranges from 70 to 90% [11]. SDE is a particularly important performance factor in space. Due to the long distances involved — several thousand kilometers — fewer photons reach the detector. For this reason, every additional percentage point of the SDE reduces the required transmitting power. The addition of an optical mirror beneath the nanowire has resulted in the attainment of SDE values up to 99.5% [3].

In this instance, a gold mirror cavity was inserted beneath the niobium-titanium nitride (NbTiN) detector. In contrast, a distributed Bragg reflector (DBR) was coated onto a molybdenum silicide (MoSi) detector, resulting in an SDE of 98% [12].

When utilizing the DBR as a mirror beneath the nanowires, these advantages consequently result in reduced scattering losses and enhanced reflectivity. The DBR is constituted of an alternating stack of optical layers with high and low refractive indices, for example the combination of SiO₂ with the reflective index $n_{\text{SiO}_2} = 1.46$ and Ta₂O₅ with $n_{\text{Ta}_2\text{O}_5} = 2.22$ [13]. The thickness of each individual layer is equivalent to one quarter of the wavelength λ . The DBR mirror developed by the research group [12] was grown using plasma-enhanced chemical vapor deposition (PECVD), and the superconducting layer was deposited using magnetron sputtering. In this work, however, dual ion beam sputtering (DIBS) is used for both components. In comparison with PECVD and magnetron sputtering, DIBS offer a higher layer density, resulting in layers with fewer defects and lower surface roughness of less than 0.1 nm [14]. In comparison with PECVD, magnetron sputtering and DIBS are classified as physical vapor deposition (PVD). In the DIBS process, a target is sputtered with an ion beam, causing particles to be ejected and condense onto the substrate to be coated. The presence of a second ion beam source enables the substrate to be cleaned before and during the coating process. This results in an even denser and more homogeneous layer with a lower surface roughness [14][15].

3. MATERIALS AND METHODS

The coating process is responsible for the creation of intrinsic stress within the layers. These stresses subsequently cause substrate curvature, resulting in wafer bow. Consequently, further processing using lithography techniques is rendered infeasible for the fabrication of superconducting nanowires, as a prerequisite for handling in this context is a substrate surface that is as flat as possible. To reliably fabricate SNSPDs, the total wafer bow must be reduced to 2 μm . The advantages offered by DBR mirrors located beneath the nanowire are being capitalized on in this research, with methodologies for mitigating the bow being offered, thereby facilitating the subsequent processing of the wafers for the fabrication of the nanowires.

Double-sided polished 4-inch silicon wafers are utilized as the substrate, and the DBR consists of a stack of several SiO₂/Ta₂O₅ pairs. The initial surface roughness of the silicon wafers was $S_q = 0.1$ nm (RMS). A low substrate roughness is essential because the surface morphology of DIBS-deposited coatings is strongly influenced by the underlying substrate roughness and can be replicated through the multilayer stack. Since a surface roughness of approximately $S_q = 0.1$ nm was targeted for the final DBR surface, highly polished silicon wafers with sufficiently low initial roughness were selected. Figure 1 provides a visual illustration of the layered structure, showing how it should look when fully assembled with the DBR stack, the superconductive NbTiN layer and the anti-reflective coating (AR coating). The focus of this paper is the DBR stack (part 3) and the backside coating (BSC – part 5).

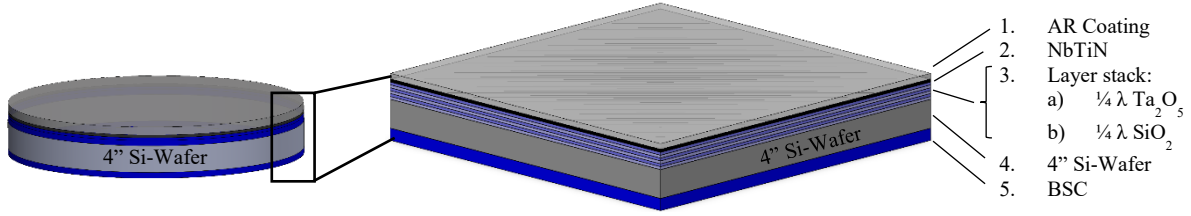


Figure 1. Graphical cross-section of the 4" silicon wafer with BSC, DBR layer stack, NbTiN layer and AR coating on top.

The layer design of the DBR structure was simulated in advance using optical simulation software. To manufacture mirrors for quantum dots [16], a design with a reference wavelength of 900 nm is simulated. For QKD [17], the design is optimized to utilize the entire telecoms range from 1310 nm to 1550 nm. The optical stack comprises several SiO_2 and Ta_2O_5 layers. The simulated reflectivity of the target wavelengths 900 nm for the quantum dots stack is 99.6% and for the wavelengths 1310 nm and 1550 nm for the telecom stacks is 99.5%.

After coating with DIBS, the curvature of the wafer is measured using a surface profilometer. The bow is then calculated using the following formula and the measured radius.

Sagitta formula

$$\text{Bow} = r - \sqrt{r^2 - l^2} \quad (1)$$

With the measured radius r and the half of the measured distance l . The following figure 2 illustrates the individual parameters.

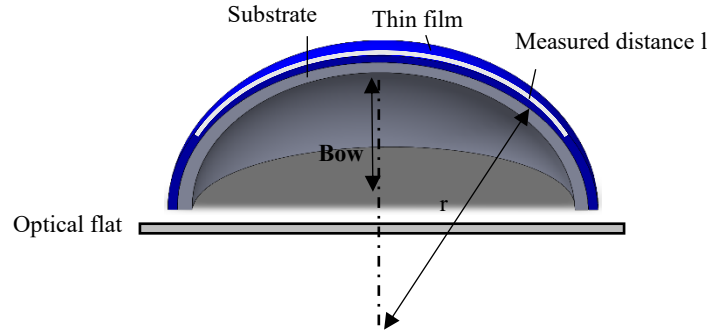


Figure 2. Illustration of the individual parameters for calculating the bow.

For calculating the stress of the layer, the Stoney equation (2) is used

$$\sigma = \frac{E}{1 - \nu} \frac{t_s^2}{6t_f} \left(\frac{1}{R_1} - \frac{1}{R_2} \right) \quad (2)$$

With the Stress σ , Young's modulus E , the Poisson ratio ν , Thickness of the substrate t_s , curvature before coating R_1 , curvature after coating R_2 and the thickness of the layer t_f . The sign indicates the type of stress when calculating stress. A positive value corresponds to tensile stress (Figure 3 left), while a negative value indicates compressive stress (Figure 3 right). Figure 3 shows the comparison and resulting effects of the two different types of stress on the wafer.

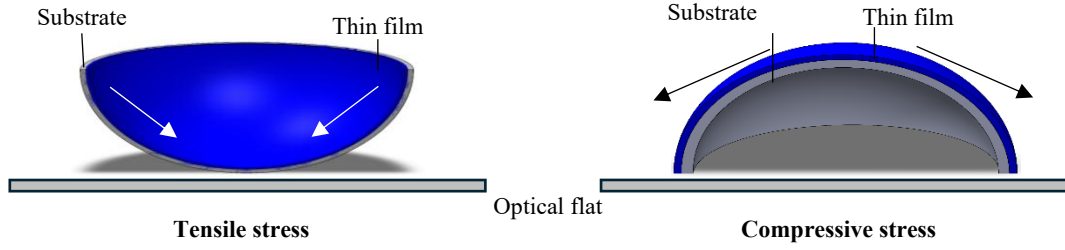


Figure 3. Comparison of the bow behavior between tensile stress (left) and compressive stress (right).

Various methods are used to compensate for the curvature, including heat treatment and backside coating. To protect the surface of the DBR mirror during the BSC process, a layer of FirstContact polymer was applied to the wafer using spin coating. After the process the polymer can be peeled off without leaving any residue. To reduce the bow, the wafer is heated in a furnace. For this process, the substrate is annealed at 400 °C for 10 hours. Measurements are carried out using techniques such as atomic force microscopy, beam profilometer or photo spectrometry after the treatments.

4. RESULTS AND DISCUSSION

The absorption of photons in the NbTiN nanowire for the layer stack shown in Figure 1 was simulated using the Lumerical simulation software, with the results presented as a function of the AR coating materials and its thickness (Figure 4). Therefore, an absorption rate of 99.9% can be achieved by choosing the right layer design of the AR coating.

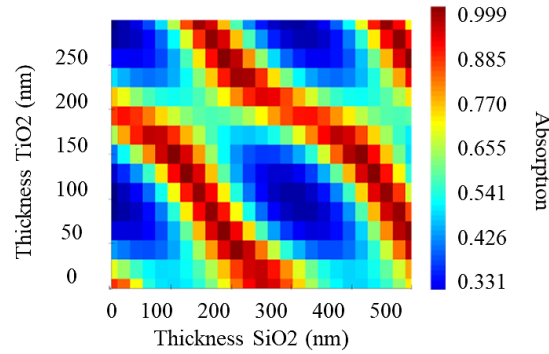


Figure 4. Simulated absorption efficiency of a NbTiN nanowire under 900 nm illumination on a DBR with bi-layer anti-reflection coating ($\text{SiO}_2 / \text{TiO}_2$).

The reflectivity of the DBR was simulated using optical simulation software with an angle of 8°. To achieve this, a layered structure consisting of Ta_2O_5 and SiO_2 was selected, resulting in a reflectivity of 99.6 % at a wavelength of 900 nm (Figure 5 blue graph) and a simulated thickness of 2.5 μm . Reflectance was measured using a photon spectrometer at an angle of tilt of 8°. The reflectance at 900 nm was found to be 99.6% $\pm$ 0.1. The measured curve of the reflectance can be seen in the red graph of figure 5. The deviation in the measured curve within the 1050 – 1150 nm range is due to measurement inaccuracy of the Photon RT device in the infrared range which leads to a broadening of the peaks and valleys.

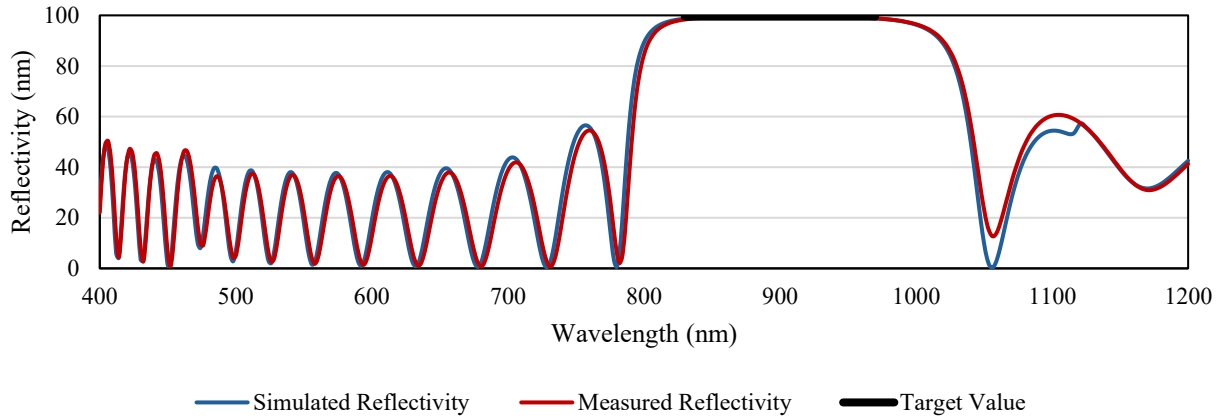


Figure 5. Optical simulation and measurement of the 900 nm DBR mirror reflectivity with a tilt of 8° . Blue: simulated reflectivity, black: target values and red: reflectivity measurement.

For the simulation of the telecommunications range, the telecommunication DBR mirrors were designed and optimized to achieve a reflectivity greater than 99.5% over the wavelength range from 1310 to 1550 nm. The maximum reflectivity of 99.9 % is found at the center of the range, at a wavelength of 1414 nm, red spectra graph in figure 6. Comparison of the measured and simulated spectra indicates a small shift of the measured spectrum toward longer wavelengths. Consistent with this shift, the measured reflectivities at 1310 and 1414 nm are $98.1 \pm 0.1 \%$ and $99.7 \pm 0.1 \%$, respectively, which are lower than the simulated values of 99.5% and 99.9%. Conversely, at 1550 nm, the measured reflectivity is $99.6 \pm 0.1 \%$, slightly higher than the simulated value of 99.5%. These deviations from the simulated design could be explained by measurement inaccuracies, thickness inhomogenities of the layer and the change in the angle of incidence caused by the $350 \mu\text{m}$ bow after the coating. Due to the large number of layers, even a slight variation in the thickness of each layer has a significant impact on the optical stack. Consequently, even a slight increase in the thickness of a layer in the nanometer range causes the reflectivity window to shift to the right. The simulated thickness of the whole layer stack is $5.1 \mu\text{m}$.

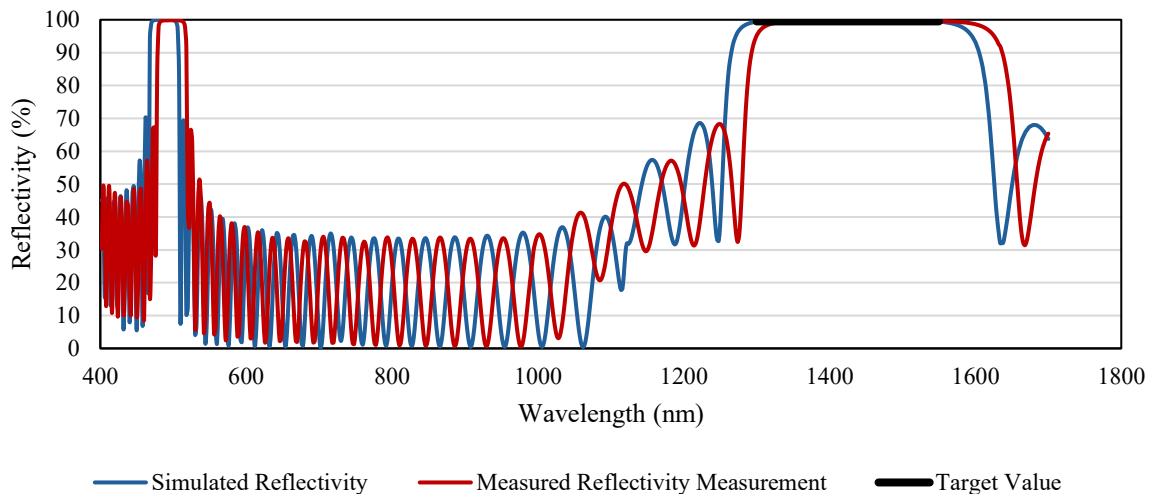


Figure 6. Optical simulation and measurement of the telecom DBR mirror reflectivity with a tilt of 8° . Blue: simulated reflectivity, black: target values and red: reflectivity measurement.

The following stress reduction experiments were conducted on the mirror at 900 nm shown in Figure 5. The DBRs are measured using a beam profiler after front-side coating (FSC). The bow was then calculated using Formula 1. As the curvature is still very high for the 900 nm DBR layer stack with a bow value of 160 μm , the wafer is annealed to reduce it. It was found that the reduction in bowing after annealing was minimal to 141 μm . The next step is therefore to do the back side coating (BSC) with the same design as for the front side. The FSC generates a compressive stress in the layer, which acts on the wafer. To counteract this, a layer with an opposing stress behavior is applied to the backside. This reduces the bow from 141.4 μm to 18.0 μm . A final annealing step was carried out to reduce the bow from 18.0 μm to 1.2 μm (Figure 7 and 8). Figure 7 shows the beam profile measurement of the wafer with a length of 80 mm. The profile indicates that the wafer is under compressive stress. This is advantageous for further applications involving the superconductive state. Tensile stress in the layer increases the lattice spacing. This can weaken electron-photon interactions, which are important for forming Cooper pairs. Conversely, compressive stress often reduces the lattice spacing, enhancing the coupling between electrons and lattice vibrations [18]. Figure 8 illustrates the bow reduction depending on the different treatments.

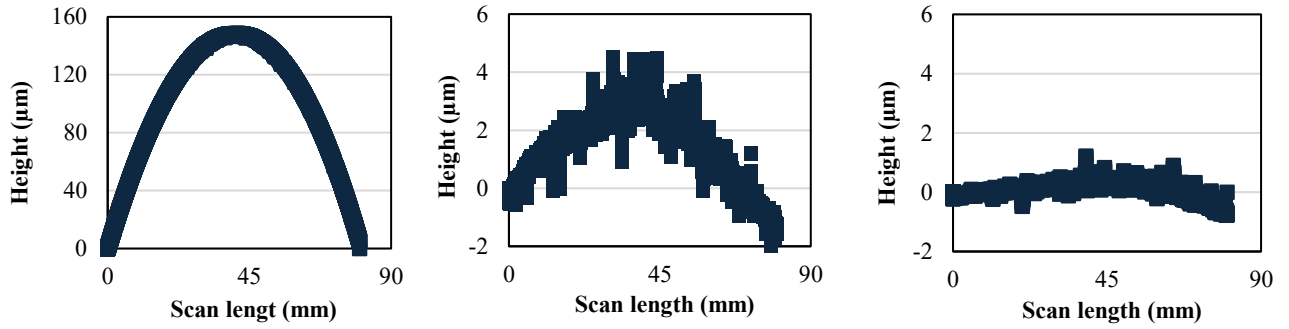


Figure 7. Bow behavior of the 900 nm DBR layer stack after different treatments. Left: after FSC, middle: after BSC, right: after final annealing.

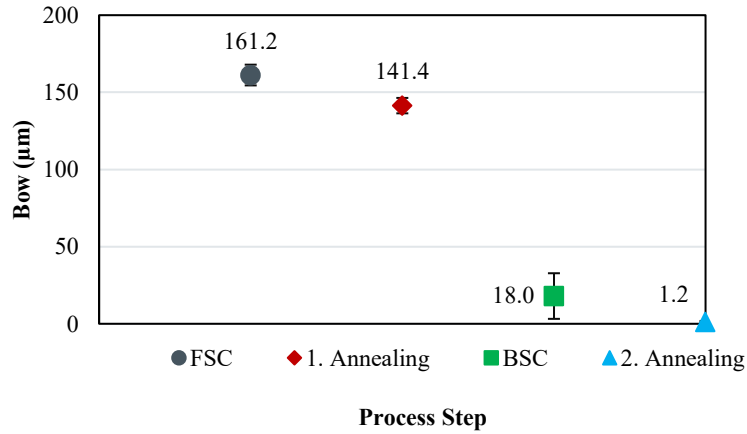


Figure 8. Bow comparison with different treatments of the 900 nm DBR layer stack.

Following the coating process and beam profile measurements, the surface roughness of the 900 nm DBR layer stack was measured. Figure 9 shows the atomic force microscope (AFM) image of the layer stack, which has a root mean square of $S_q = 80$ pm. This demonstrates the extremely low surface roughness of DIBS layer.

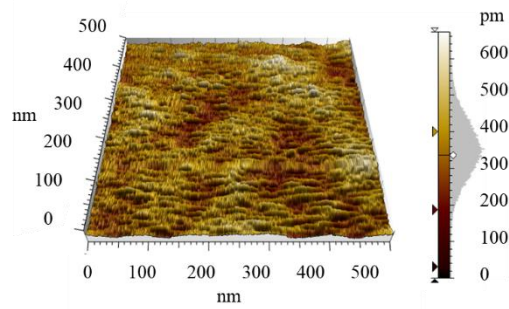


Figure 9. AFM Measurement of the 900 nm DBR layer stack with an RMS surface roughness of $S_q = 80$ pm.

5. CONCLUSION AND FUTURE WORK

In this study, DBR mirrors were coated using DIBS to minimize scattering losses by achieving low defect, homogeneous low-roughness layers, thereby increasing the efficiency of the SNSPD. The reflection of the layer stacks was 99.6 % for the 900 nm DBR stack and 99.5 % for the telecom range which was achieved with minimum deviation from the target values. The roughness study also showed that the mirror surface roughness remained similar to that of the pure silicon wafer. After the coating process, it was found that the wafer warped by $160\text{ }\mu\text{m}$ due to the build-up of compressive stresses. In order to enable further processing for lithographic applications, this bow must be compensated for. Various methods are being tested on wafers to this end. It has been demonstrated that annealing the wafer alone is insufficient to reduce the wafer bow to the target value of $2\text{ }\mu\text{m}$. However, applying an additional coating to the backside results in the bow reduction from $160\text{ }\mu\text{m}$ to $18\text{ }\mu\text{m}$. A final annealing step reduces the total stress further, bringing the bow down to a value of $1.2\text{ }\mu\text{m}$. This process enables DBR to be deposited onto the 4-inch wafer and prepares it for further processing.

Further research will involve optimizing the DBR layer stack for the telecommunications range to achieve higher reflectivity at a wavelength of 1310 nm . Additionally, the bow of the wafers with the telecom DBR will be reduced using the aforementioned processes. To test the hypothesis presented in the result section, future tests will include ellipsometer measurements and a repetition of the reflectivity measurement after bow compensation. Initial tests involving NbTiN coating are also being conducted. This enables the deposition of the layer stack at wafer level rather than just at chip level and it is also a promising option for enhancing the performance factors as SDE, DCR and timing jitter of the SNSPD.

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