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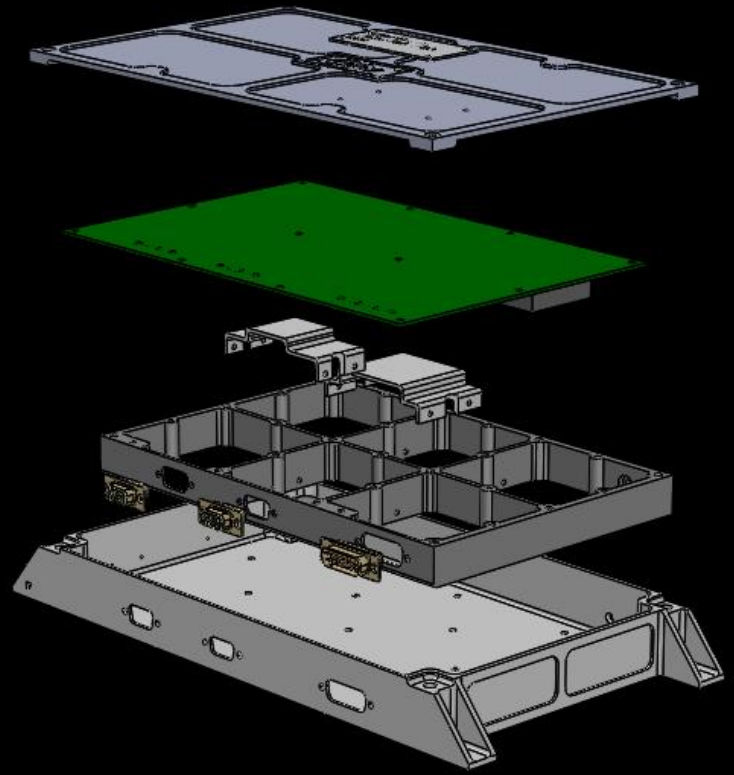
RECONFIGURABLE CO-PROCESSOR FOR SPACECRAFT AUTONOMOUS NAVIGATION



OBDP 2021
16/06/2021

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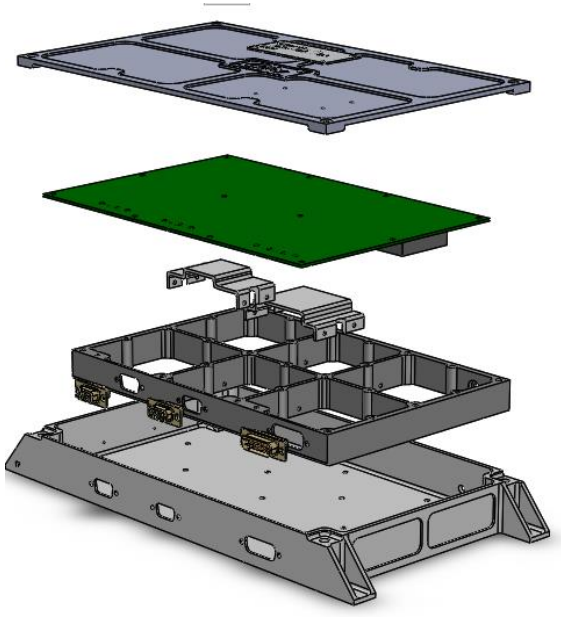
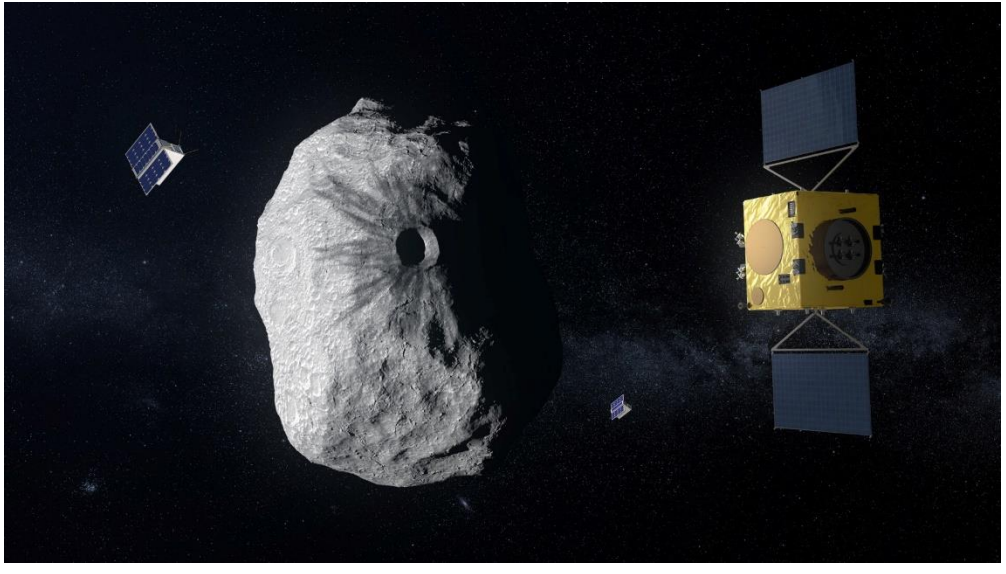


CONTEXT : HERA MISSION

- Asteroid Impact and Deflection Assessment
- DART and HERA
- Target: Dydimos Binary Asteroid
- HERA – ESA Contribution
- Spacecraft Autonomous Navigation Required



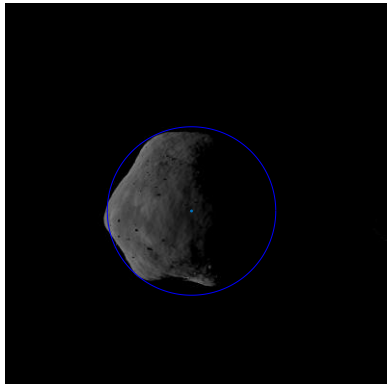
http://wwww.esa.int credit for the images on this slide

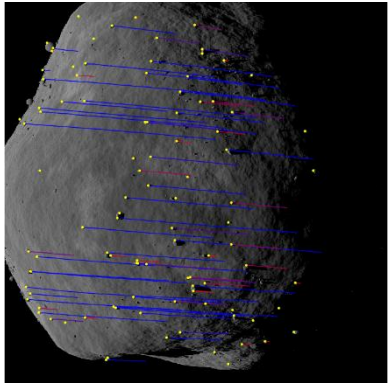
- DART – NASA contribution
  - launch 2021
  - Colission 2022
  - Kinetic impact on small body
- HERA – ESA Contribution
  - Launch 2024
  - Reaches Didymos in 2026
  - Detailed post impact survey
  - Demonstration of novel technologies

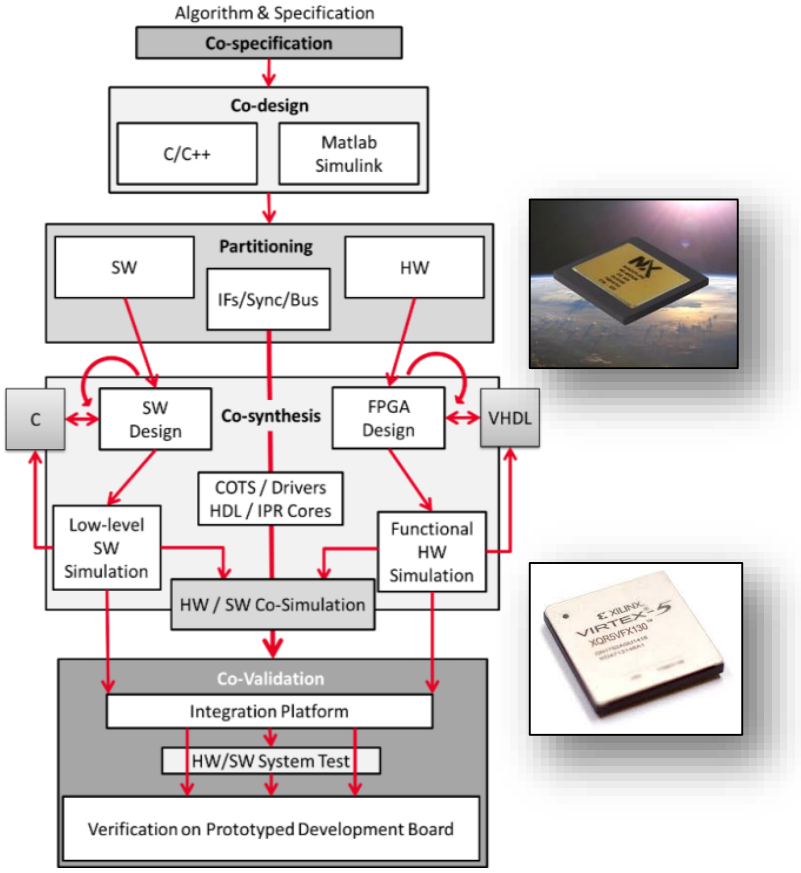
CONTEXT : AUTONOMOUS NAVIGATION

- Avionics unit for Image Processing on HERA S/C
- HW/SW Co-design approach for Navigation
- GNC implemented in HERA S/C OBC LEON3
- Image Processing Unit
  - 2 FPGAs: Virtex5 and NG-MEDIUM Rad-Hard FPGAs
  - Feature Tracking HW-acceleration
  - Lambertian Sphere Correlation Centroid HW-acceleration
  - Interfaces Management in FPGA

**Feature Tracking and Centroid IP functionality are also implemented in HERA S/C OBC*

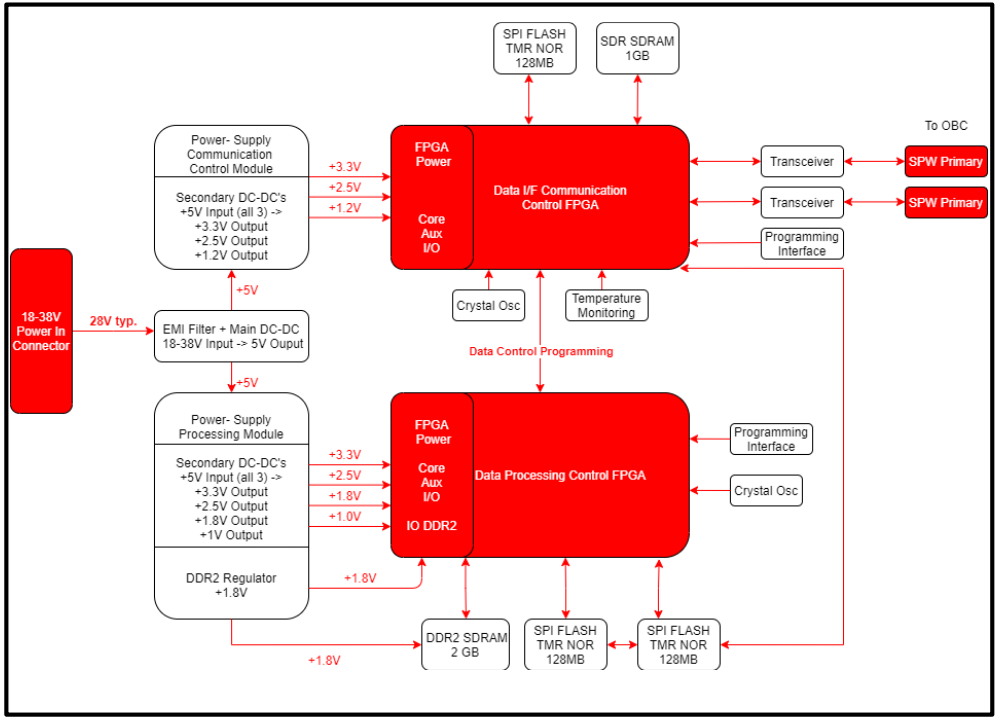






IPU CONCEPT : ELECTRONICS

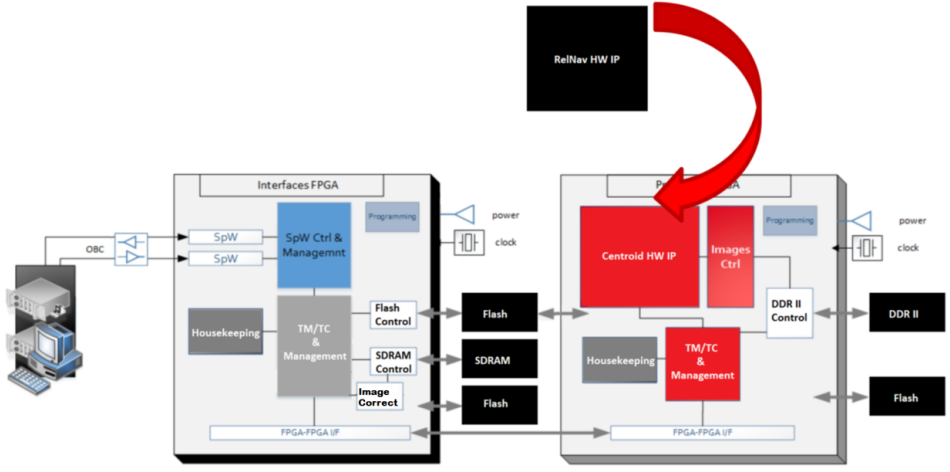
- Co-processor for Autonomous Navigation:
  - NanoXplore NG-Medium
  - Xilinx Virtex5
- Input: 28V Unregulated
- External DDR2 devoted to Virtex5
- External SDRAM devoted to NG-Medium
- 2 x SpaceWire ports – connected through transceivers
- Reconfigurable Processing FPGA
- LVDS Interlink between the two FPGAs
- Protections against failure propagation
  - External Overvoltage Protection on main DC/DC
  - Internal Overvoltage Protection on secondary DC/DCs



IPU CONCEPT : FPGA DESIGN

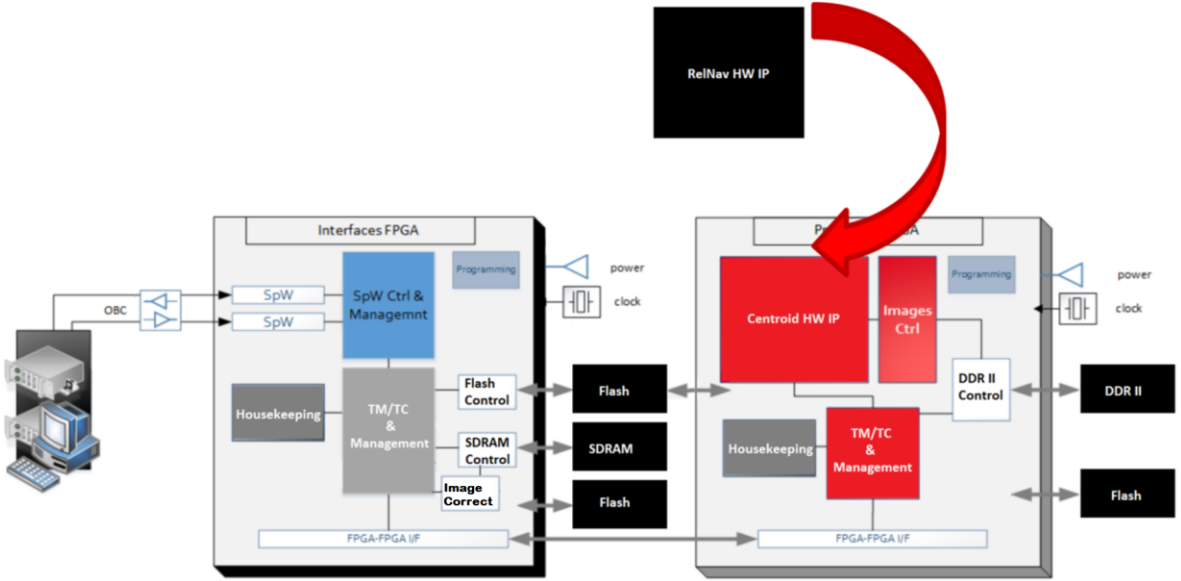
- Interfaces FPGA:
  - NG-Medium
  - Image Pre-Processing Capabilities (Camera corrections)
  - Deals with the SpaceWire interfaces of the IPU to the S/C OBC
  - Manages the reprogramming of the Processing FPGA
  - Master FPGA – allows safe reconfiguration of Processing FPGA (control over Processing FPGA is not lost in case of wrong configuration)

- Processing FPGA: Image Processing HW IP-core (high-performance & high-density SRAM-based FPGA)
  - Virtex-5QV VFX130T
  - Hosts Feature Tracking HW IP and Centroid HW IP



IPU CONCEPT : RECONFIGURATION

- Reprogramming of Processing FPGA Virtex 5
- Managed by Interfaces FPGA NG-Medium
- Scenarios:
  - Select a new bitstream from the already preloaded options in the FLASH #1 (Centroid or FeatureTracking).
  - Upload a new bitstream to the IPU that was not preloaded before launch (using FLASH #2).

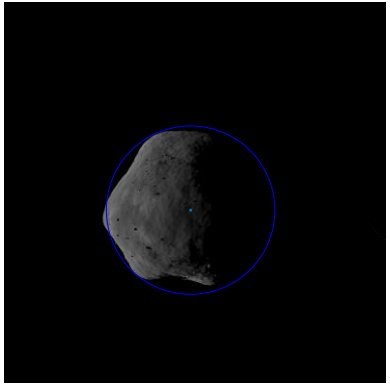


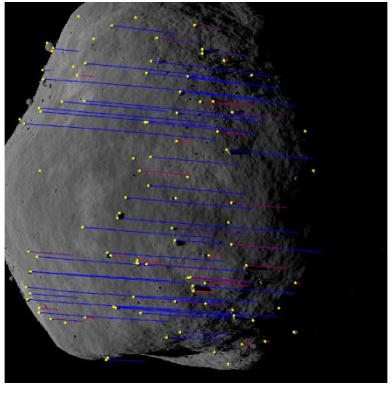
DATA PROCESSING : GNC STRATEGY

- Image Processing Techniques
  - Centroid (for distance to Didymos higher than 9.5 km)
  - Feature Tracking (for distance to Didymos less than 9.5 km)

- Implementation
  - HERA S/C OBC
    - Feature Tracking Execution Time: 10s
    - Centroid Execution Time: 9s
  - HERA IPU
    - Offloads HERA S/C OBC
    - Typical Power Consumption: 20W (Peak), 15W (Idle)
    - Execution time of HW IPs: less than 1s
    - Execution time for entire data flow inside IPU (including image correction): less than 3s

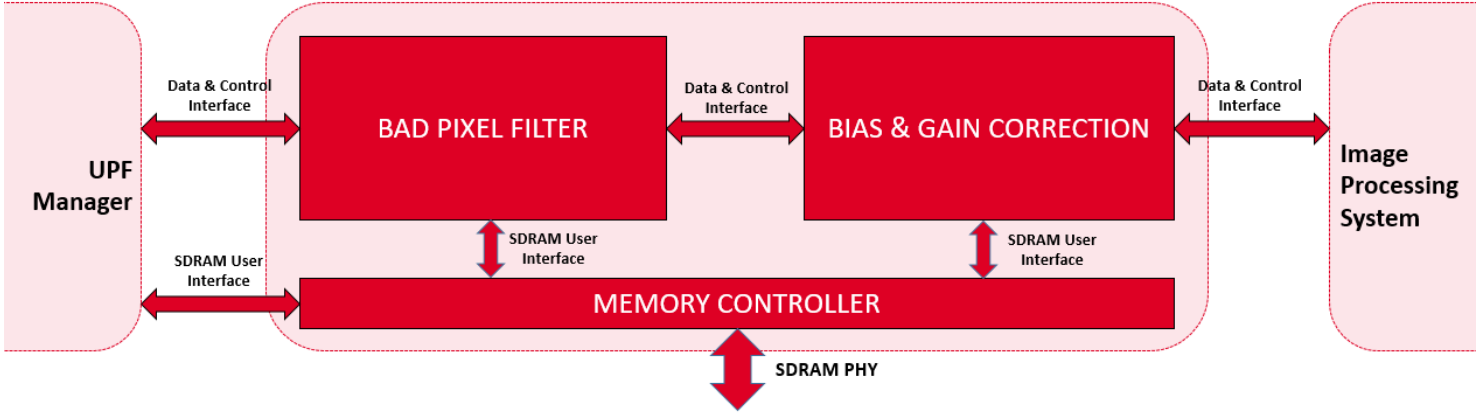
  Lower execution times (2s) can be achieved for IPU for higher FPGA design clock frequency and in case Image correction is not needed





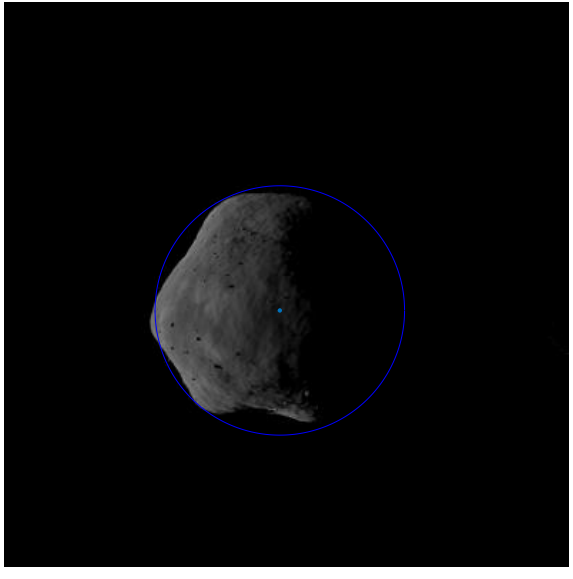
DATA PROCESSING : IMAGE CORRECTIONS

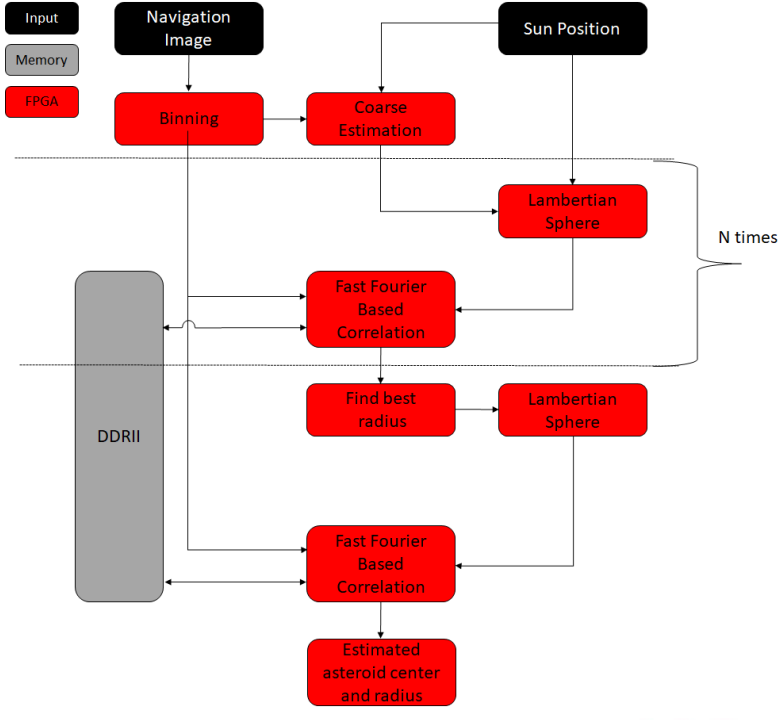
- Ussually provided by Navigation Camera
- Performed by Interfaces FPGA NG-Medium on 1024x1024 pixel images (8 bit pixel depth)
- Implemented also on Processing FPGA as back-up
- External Volatile memory SDRAM used by Interfaces FPGA
- Approach
  - Bias & Gain Correction (Pre-Processing)
  - Bad Pixel Correction (Pre-Processing)
  - Lens Distorssion Correction (Post Processing)



DATA PROCESSING : CENTROID

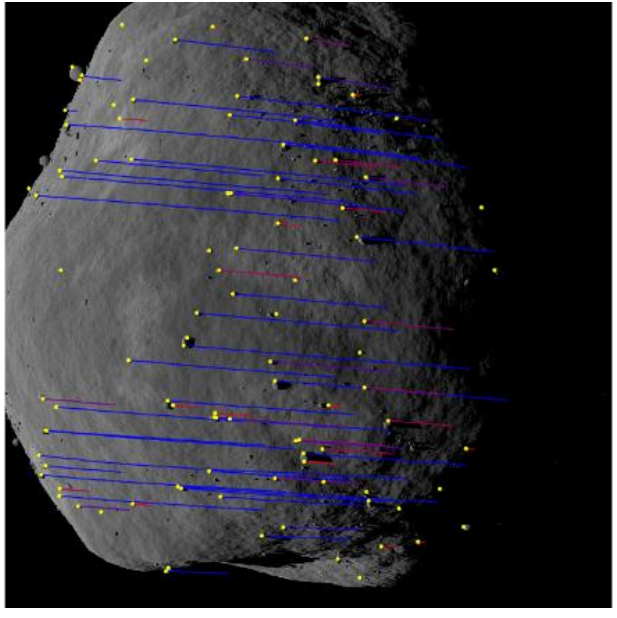
- Reduced User Interface
  - Inputs: Sun Vector, Navigation Image 1024x1024 pixels (8 bit per pixel)
  - Outputs: Asteroid Center, Estimated Radius
- External Volatile memory required
- HW IP Processing time: 900 ms

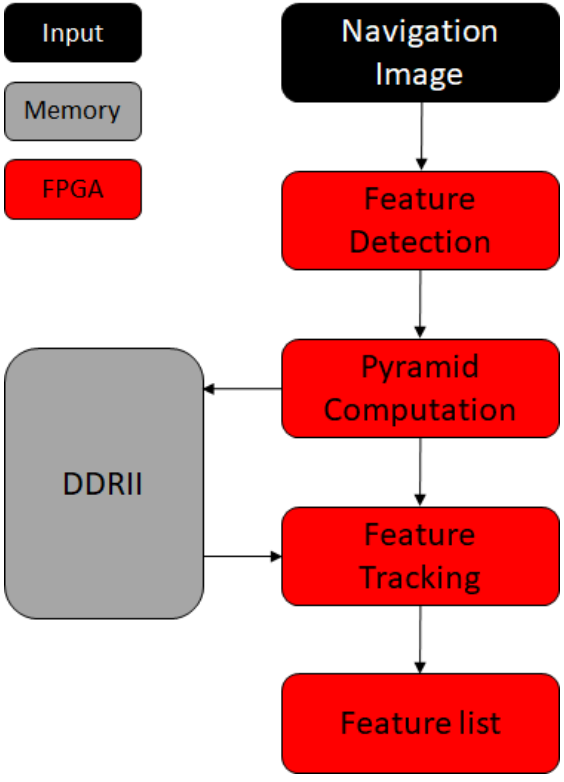




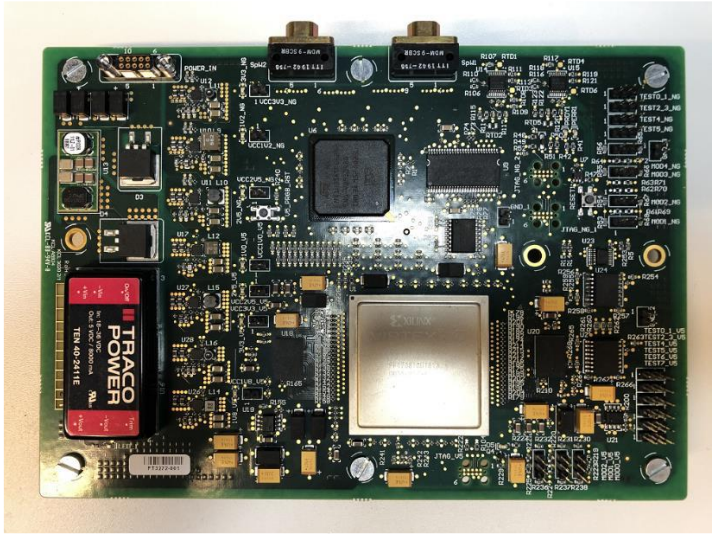
DATA PROCESSING : FEATURE TRACKING

- TRL 6 achieved in CAMPHORVNAV with different tunning
- Reduced User Interface
  - Input: Navigation Image 1024x1024 pixels (8 bit per pixel)
  - Output: 100 features
- HW IP-Core Processing Time: 120 ms
- External volatile memory required





HARDWARE : HERA IP-ICU (IPU EBB)

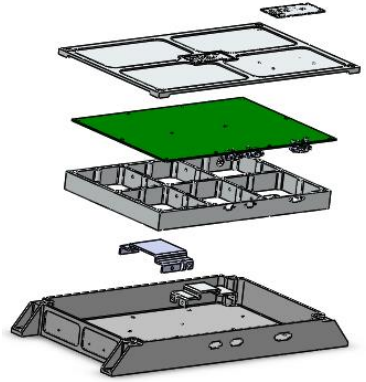


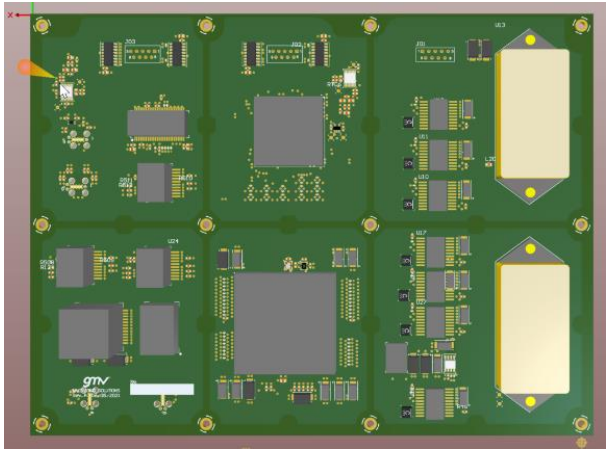
- Electronics manufactured 2020 – Model is currently used for VHDL Development
- Physical Information
  - 140x200mm large
  - 12 layers stack-up
  - Polyamide Arlon 35N, designed for sequential lamination
  - PCB Design mostly ECSS Compliant
- IP-ICU EBB Fully representative to HERA mission needs in terms of function, interface and processing power.
  - 2 x SpaceWire I/Fs providing >40 Mbps (autostart/ autodetect functionality included)
  - External volatile memory (SDRAM) allocated to UIF for Navigation Image Reconstruction/ Pre-Processing
  - Processing Capabilities by means of UPF Virtex-5 & allocated external volatile memory (DDR II)
  - Reprogramming Capabilities (Centroid & Feature Tracking IPs can be stored prior launching into one flash memory; second flash memory allocated to Virtex-5 can be let for in-flight reprogramming with bitstreamm received from ground)
  - 28 VDC unregulated bus

HARDWARE : EM AND HIGHER TRLS

Evolution of IP-ICU EBB into fully functional EM

- Electronics
  - Replacement of passive components. Chosen components with packages in dimensions for the EM model based on the target space graded components.
  - Full compliance to ECSS of the PCB design.
  - Some critical electronic components are maintained with respect to the EBB (FPGAs, transceivers)
  - DC/DCs and EMI Filter are replaced with exact commercial counterparts from same vendor as for EQM (representativeness for space grade components) => Upgrade of some EBB parts while maintaining critical ones in order to be as realistic as possible to what will be used in EQM
  - Removal of jumpers, switches, push-buttons
  - Removal of LEDs and transistors that drive the LEDs
  - 240 mm x 160 mm Layout
- Mechanical Integration
  - Metallic enclosure box with stiffeners
  - Metallic heathsinks for some of the components
  - Envelope 350 x 180 x 40 mm





Evolution into flight hardware EQM/PFM

- Only RHA components
- ECSS soldering
- Environmental qualification campaign
- PFM completion August 2022

CONCLUSIONS

- Two FPGAs architecture for Image Processing Board, validated at TRL 4/5 already.
- Reliability assured by means of separating functionalities between two FPGAs.
- Reprogramming functionality managed by Master FPGA NG-Medium for keeping control over the unit in case wrong reprogramming of the Processing FPGA Virtex-5QV
- SpaceWire CCSDS/PUS for reusability and integration
- Image correction techniques can be used by IPU in case navigation camera does not provide these capabilities
- Compact dimmensions and power consumption values that allow simple integration into satellite avionics architecture

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THANK YOU

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