

Development of a High Photon Efficiency Optical Modem for the Ground Segment Based on Multichannel TDC and DTC

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ABSTRACT

This paper presents the preliminary development of a high photon efficiency (HPE) modem for the ground segment, based on multi-channel time-to-digital converter (TDC) and digital-to-time converter (DTC) techniques. The work is carried out within the High Photon Efficiency Ground Segment Modem (HPE-GSM) European Space Agency (ESA) activity. It addresses the need for flexible and power-efficient optical communication solutions for future deep-space and long-range free-space optical (FSO) links. The proposed modem is intended for pulse position modulation (PPM)-based communication and is being developed as a ground-segment system evolving from a TRL4 Prototype toward a TRL5 Engineering Model (EM) aligned with Consultative Committee for Space Data Systems (CCSDS) optical communication standards.

The activity builds on the previous ESA-supported TiPiPLas proof-of-concept activity, in which a real-time differential PPM transceiver was demonstrated using DTC-based pulse generation and off-the-shelf time-tagger-based reception. That implementation validated the feasibility of using digital delay lines as DTC elements and event-timing hardware as TDC elements, but remained limited by receiver dead time, achievable throughput, integration level, and compatibility with standardised optical communication frameworks. These limitations are addressed in HPE-GSM through a more integrated modem architecture based on dedicated multi-channel TDC and DTC techniques and support for advanced coding techniques, including serially concatenated pulse position modulation (SCPPM).

The paper presents the architecture and experimental evaluation of an early TRL4 Prototype, including timing calibration, pulse-position accuracy, and preliminary bit error ratio (BER) measurements. The prototype supports configurable PPM orders and demonstrates operation with slot widths down to 31 ps. The paper therefore describes both the current experimental results and the implementation approach guiding its evolution toward the TRL5 EM and an integrated C-band terrestrial FSO subsystem with pointing, acquisition and tracking (PAT).

The final modem is intended to support configurable PPM formats and alignment with CCSDS 141.0-B-1 and 142.0-B-1, targeting bit rates up to 800 Mbit/s in custom operation and approximately 300 Mbit/s in the fully CCSDS-compatible configuration.

Keywords: high-photon-efficiency, pulse position modulation, time-to-digital conversion, digital-to-time conversion, free-space optical communication, optical ground segment, CCSDS, deep-space optical communication

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1. INTRODUCTION

Deep-space missions require communication links capable of returning increasing volumes of scientific and operational data over interplanetary distances. Existing radio frequency (RF) links are increasingly constrained by available bandwidth and link budget, whereas FSO communication offers substantially larger information capacity for long-range links. Recent developments in deep-space optical communication, including NASA's deep space optical communications (DSOC) demonstration and the associated ESA ground infrastructure,¹ confirm the feasibility of HPE optical links for future exploration missions.² For photon-starved links over very large distances, PPM-based direct-detection communication is particularly attractive because it combines high receiver sensitivity with low average transmitted power.

European capability in HPE optical communication is progressing from experimental ground infrastructure toward dedicated modem implementations. ESA-supported activities have demonstrated CCSDS-compatible HPE modem technology and its integration into deep-space optical communication demonstrators.³ Development of an independent European ground-segment modem is therefore a logical next step toward operational CCSDS-compliant optical links for future lunar and deep-space missions. The same technology is also relevant to secure governmental and defence-related communication, where narrow optical beams, immunity to radio-frequency interference, and high power efficiency provide advantages for resilient long-range links.⁴

The feasibility of this approach has been established by the authors in a series of previous studies. Event-timer-based reception was demonstrated for high-order differential pulse position modulation (DPPM) with slot widths down to 50 ps.⁵ A dedicated programmable-delay-line transmitter subsequently demonstrated transmitted reference pulse-position modulation (TR-PPM) generation using digital delay lines (DDLs) as DTC elements.⁶ The optical applicability of the concept was demonstrated using 512-TR-PPM over a 20 km C-band fibre-optical link.⁷ Timing errors associated with jitter and clock drift, together with their mitigation by Gray and Reed–Solomon coding, were analysed in.⁸ These developments culminated in a reconfigurable real-time transceiver combining a DDL-based DTC transmitter with a streaming event timer used as the TDC receiver,⁹ developed as part of the ESA TiPiPLas activity. The latter system demonstrated practical real-time data transmission, but its performance was limited by the dead time, physical size, control interface, and data-transfer architecture of the general-purpose event timer. The concept was further extended to a hybrid analogue radio-over-fibre link using PPM, demonstrating transmission through a 20 km optical-fibre segment and a 6.6 GHz wireless link.¹⁰

Time-domain processing also enables applications extending beyond point-to-point communication. Continuous event recording can combine optical communication with laser ranging and sensing within a common timing architecture, enabling integrated sensing and communication (ISAC)-type functionality for space systems.¹¹ Such capability is relevant to optical ground stations, satellite laser ranging, space-domain awareness, tracking, and other applications where communication and precise event timing must coexist.

Building on these results, the HPE-GSM activity targets the development of a dedicated ground-segment PPM modem based on high-rate and high precision TDC and DTC technologies. The final system is intended to implement the physical-layer, synchronization, and channel-coding functions defined by CCSDS 141.0-B-1¹² and 142.0-B-1¹³ and to operate with a C-band FSO subsystem. The development targets data rates up to 833 Mbit/s in custom operation and approximately 333 Mbit/s in a fully CCSDS-compatible configuration.

This paper presents the architecture and experimental evaluation of an early beta design of the HPE-GSM Technology Readiness Level (TRL) 4 Prototype. In contrast to the earlier system, where an external general-purpose event timer was used for PPM reception, the given prototype integrates dedicated timing, pulse-generation, calibration, control, and data-transfer functions in a single modem platform. The modem prototype is not yet fully CCSDS compliant; rather, it serves to validate the timing-centric architecture and the performance improvements required for the subsequent TRL5 Engineering Model.

2. TIME-DOMAIN IMPLEMENTATION OF PPM

2.1 Pulse-position Modulation

PPM is particularly well suited to photon-limited optical links because information is encoded in the temporal position of short pulses. For an M -ary PPM waveform, a single transmitted pulse represents $\log_2 M$ information

bits, allowing a low duty cycle and a high peak-to-average optical power ratio. The timing nature of PPM also enables an implementation in which transmitted and received information is processed directly in the time domain rather than through continuous broadband waveform sampling.

At the transmitter, a DTC determines the temporal position of each pulse, while at the receiver a TDC measures the arrival time of detected events. This approach is particularly attractive for picosecond-scale PPM, where the information-bearing quantity is the pulse position rather than its amplitude. As a result, the required modem bandwidth can be handled through precise event timing instead of relying on very-high-speed analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The achievable data rate is therefore determined primarily by timing resolution, receiver dead time, supported PPM order, and the minimum guard interval between adjacent pulses.

2.2 TDC-based PPM reception

In a TDC-based PPM receiver, the absolute arrival time of each detected pulse, referred to as a time tag t_k , is measured relative to the time reference of the TDC. For a slot width Δ and an M -ary PPM symbol, the ideal arrival time can be expressed as

$$t_k = t_{0n} + k\Delta, \quad k = 0, \dots, M-1, \quad (1)$$

where t_{0n} denotes the expected start time of the n -th subframe and k is the transmitted pulse position. To prevent pulses in adjacent symbols from occurring too close to each other, a guard interval t_g is inserted between consecutive symbols. The symbol interval together with the guard interval forms a subframe. The start time of the n -th subframe can therefore be expressed as

$$t_{0n} = n(M\Delta + t_g). \quad (2)$$

In practice, however, the estimated value of t_{0n} must be continuously adjusted to compensate for timing jitter and relative clock drift.⁸

The achievable slot width is determined by the combined timing uncertainty of the complete receive path, including detector and front-end jitter, TDC measurement uncertainty, synchronization error, and residual timing offsets. If the timing uncertainty becomes comparable to the slot width, an event may be assigned to an adjacent slot, resulting in a symbol error. Consequently, high-order PPM with narrow slots requires both high timing resolution and accurate synchronization. Increasing the PPM order M enables a trade-off between data rate and energy efficiency of the optical link.⁵

The PPM demodulator therefore determines the position index k by dividing the difference between the measured time tag t_k and the expected subframe start time t_{0n} by the slot width and rounding the result to the nearest integer:

$$k = \left\lfloor \frac{t_k - t_{0n}}{\Delta} + \frac{1}{2} \right\rfloor. \quad (3)$$

In addition to timing resolution, the minimum spacing between consecutive measurable events is an important receiver parameter. The TDC dead time limits the maximum event rate and can therefore constrain the achievable data throughput independently of the single-shot timing resolution. This limitation can be mitigated by selecting a sufficiently large guard time t_g between consecutive symbols; however, increasing t_g directly reduces the achievable data rate. For high-rate TDC-based PPM reception, an appropriate trade-off between timing precision, receiver event rate, and guard time is therefore required.

2.3 DTC-based PPM generation

At the transmitter, a DTC performs the inverse operation by converting the digital PPM symbol into an accurately positioned output pulse, with the required pulse position determined according to (1). Picosecond-scale pulse positioning can be implemented by combining a coarse digital timer with a programmable fine-delay element. The coarse timing stage defines the approximate pulse position within the symbol interval and has a significant impact on the maximum event rate, while a digital delay line provides the fine timing adjustment required to achieve the desired slot width.

Table 1. Comparison of the preliminary modem and the HPE-GSM prototype.

Parameter	Preliminary design ⁹	HPE-GSM prototype
Receiver architecture	ESTT 7 Series external event timer	Integrated TDC-based receiver
Modulation schemes	PPM, TR-PPM and DPPM	Configurable PPM
Demonstrated modulation	DPPM	PPM
PPM order	2 ... 512	4 ... 1024
Minimum demonstrated slot width	40 ps	31 ps
DTC timing granularity	10 ps	10 ps
Receiver single-shot RMS resolution	2.2–2.3 ps	25 ps
Receiver minimum event spacing	40 ns	1 ns
Maximum continuous event rate	20 MEPS	Up to 238 MEPS
Transmitter architecture	FPGA and DDLs	FPGA and DDLs
Maximum precision delay	10.45 ns	10.23 ns DDL range
Maximum coarse delay (symbol length)	655.35 μ s	655.36 μ s
Pulse width	150 ps in reported tests	2.4–12.63 ns
Maximum packet length	8000 symbols	16000 symbols
Host interface	USB 3.0 for separate TX and RX	Integrated USB 3.1
Time-tag-to-PPM demodulation	PC-based software	PC-based software
Calibration	Manual	Integrated TX/RX
Practical demonstrated bit rate	Approximately 10 Mbit/s	To be evaluated
Theoretical useful bit rate	Around 149 Mbit/s	Around 800 Mbit/s ($M = 16$, $\Delta = 0.25$ ns, $t_g = 1$ ns)
CCSDS compatibility	Not compliant	Compliance with some modes but not yet implemented

The practical accuracy of such a transmitter is affected by delay-line granularity, differential and integral non-linearity, clock uncertainty, and fixed propagation delays in the signal path. Calibration is therefore required to establish the relationship between the programmed delay values and the actual generated pulse positions. The resulting correction can subsequently be applied to reduce systematic position errors across the complete PPM range.

An important feature of the time-domain implementation is that the information is carried by the position of the pulse edge rather than by its duration. The generated pulse width may therefore be considerably longer or shorter than the PPM slot width in custom operating modes, provided that the pulse position can be unambiguously determined at the receiver. This allows fine temporal positioning to be achieved without requiring equally short electrical pulses.

3. DESIGN OF PPM MODEM PROTOTYPE

The HPE-GSM TRL4 Prototype represents a substantial redesign of the previously demonstrated time-tagger-based PPM transceiver.⁹ In the earlier implementation, a dedicated DTC-based transmitter was combined with an external Eventech ESTT 7 Series event timer acting as the TDC-based receiver. The transmitter employed a field-programmable gate array (FPGA), a coarse timing stage, and programmable DDLs with a 10 ps timing granularity, whereas the received events were continuously time-tagged by the external event timer and transferred through Universal Serial Bus (USB) 3.1 to a personal computer (PC) for software demodulation. The event timer provided a high single-shot timing resolution of approximately 2.2–2.3 ps RMS, but its 40 ns dead time imposed a fundamental limitation on the achievable event rate. Although a theoretical data rate of 149 Mbit/s was obtained for 512-DPPM with a 40 ps slot width, the practically demonstrated real-time data rate was approximately 10 Mbit/s, primarily due to the receiver architecture and host-side processing limitations.

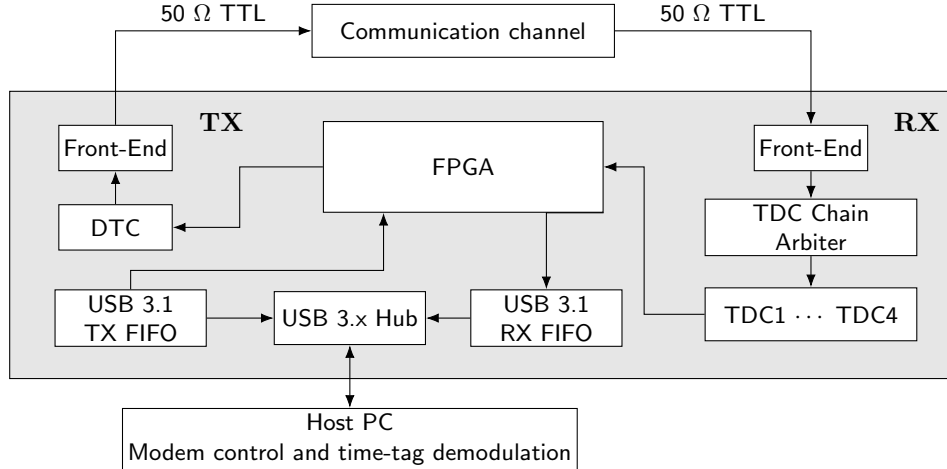


Figure 1. Block diagram of the PPM modem Prototype (beta) used in the experiments.

The block diagram of the modem Prototype is shown in Figure 1. The TRL4 Prototype retains the time-domain principle of DTC-based pulse generation and TDC-based reception, while integrating these functions into a dedicated PPM transceiver architecture. As summarized in Table 1, the Prototype supports configurable PPM orders from 4 to 1024, a minimum programmable slot width of 10 ps, pulse widths from 2.4 to 12.63 ns, and packets of up to 16000 symbols. Its receiver has a specified single-shot RMS resolution of 25 ps and supports a minimum input pulse spacing of 1 ns, with a minimum continuous event spacing of 4.2 ns. Consequently, compared with the 40 ns dead time of the previous event-timer-based receiver, the new architecture trades part of the excessive single-shot timing precision for substantially higher event throughput and tighter system integration. Transmitter and receiver calibration, PPM demodulation, time-tag acquisition, configuration, and data transfer are integrated within a common hardware and software environment accessible through a USB 3.1 interface and a dedicated application programming interface (API). The Prototype therefore represents an intermediate TRL4 implementation intended to validate the architecture and performance improvements required for the subsequent CCSDS-aligned HPE-GSM modem, while not yet providing full CCSDS compliance.

4. EXPERIMENTAL EVALUATION OF PROTOTYPE

4.1 Experimental setup

For early evaluation of the PPM modem prototype performance, two similar modem prototypes were connected "back to back". The setup diagram is shown in Figure 2. Modems are controlled from single a PC connected over two USB 3 cables to the modems. A digital phosphor oscilloscope (DPO) is used to evaluate the shape and stability of the transmitted waveform.

4.2 Prototype configuration and measurement procedure

Both transceivers were controlled from a common PC through independent USB 3.0 interfaces. The transmitter generates the PPM waveform using a combination of coarse timing and a programmable DDL, while the receiver records the arrival times of the input pulses using the integrated TDC. The prototype permits independent configuration of the PPM order, slot width, transmitted pulse width, packet length, and receiver input threshold. During the measurements, the transmitting modem was configured to generate a sequence of known PPM symbols. The corresponding electrical waveform was applied directly to the input of the receiving modem. The receiver registers the leading edge of each pulse and stores the resulting time tags. After the specified number of events has been acquired, the recorded time tags are transferred to the host computer and converted into PPM symbol values. The recovered symbol sequence is subsequently compared with the transmitted data to obtain the BER. The prototype software also provides access to the raw time tags independently of the PPM demodulator. This functionality was used for the timing accuracy and calibration measurements presented below. For each

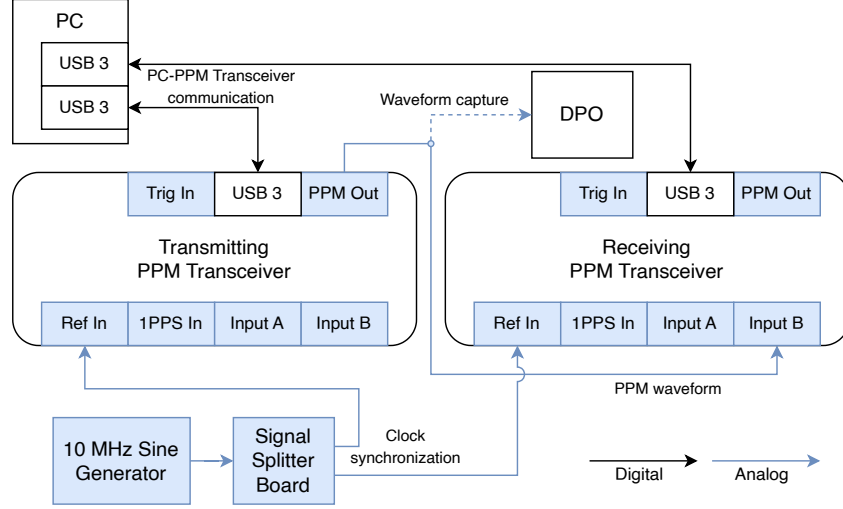


Figure 2. Experimental setup block diagram.

transmitted pulse position, the measured time tag was compared with its theoretically expected position. The resulting time deviation was used both for evaluation of the timing distribution and for adjustment of the transmitter calibration parameters. The receiver input threshold and timing offsets were adjusted before each measurement series. For measurements with relatively wide slots, the transmitter and receiver could operate from their internal timing references. For slot widths below approximately 2 ns, both units were synchronized to the same external 10 MHz reference in order to suppress relative clock drift.

4.3 Timing calibration and pulse-position accuracy

For slot widths of several nanoseconds, the accumulated timing errors of the independent transmitter and receiver clocks remain sufficiently small for reliable symbol discrimination. At sub-nanosecond slot widths, however, relative clock error and systematic non-linearity of the transmitter delay path become comparable with the slot duration. Therefore, the two modem units were locked to a common 10 MHz reference and the transmitter timing path was calibrated before the measurements. The calibration procedure consists of sequentially transmitting all available pulse positions and recording their measured arrival times at the receiver. The deviation of every measured position from its ideal value is then evaluated. Three principal systematic components can be distinguished: incorrect DDL scaling, an error in the coarse clock-related delay, and a common position offset. Representative examples are shown in Figure 3. Adjustment of these parameters minimizes the systematic position error over the complete PPM range.

The residual timing uncertainty after calibration was evaluated from the distribution of measured pulse positions. Figure 4 shows the persistent plot from DPO and distributions obtained for $M = 4$ and a slot width of $\Delta = 2.4$ ns. The measured time tag deviation distribution has an approximately Gaussian central region with an estimated RMS timing spread of about 33 ps. This confirms that, for the selected configuration, the combined transmitter and receiver timing uncertainty is considerably smaller than the slot width and therefore provides sufficient timing margin for reliable PPM symbol discrimination even if transmitted pulses have relatively slow slopes.

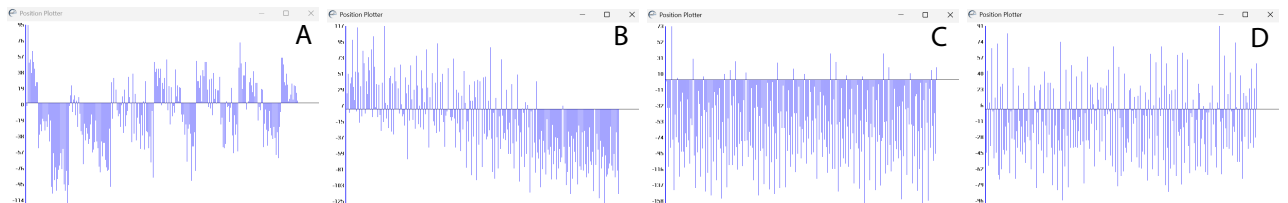


Figure 3. Position calibration bar graph. A:DDL offset, B:clock offset. C:time offset, D:optimal calibration

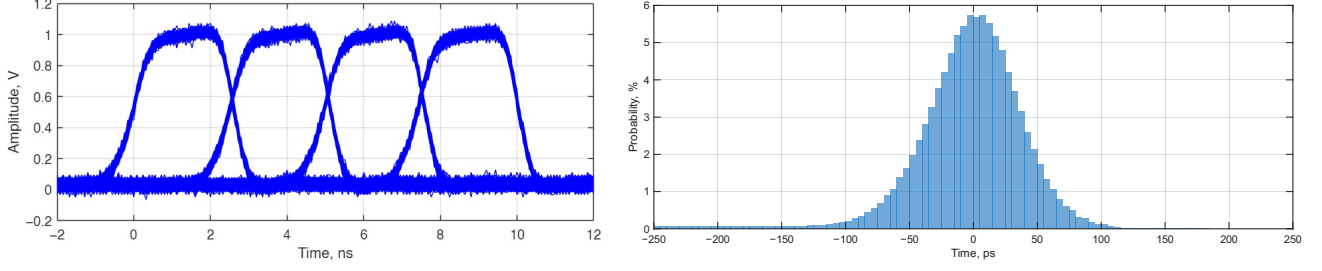


Figure 4. Persistent plot of transmit waveform and deviation distribution in the 4-position transmission at slot width 2.4 ns.

4.4 BER performance

The BER performance of the Prototype was evaluated using $M = 256$ PPM. Both the transmitting and receiving modems were synchronized to the same external 10 MHz reference clock. For each tested slot width, a sequence containing 10^7 information bits was transmitted and the demodulated sequence was compared directly with the original data. Figure 5 shows the measured BER for configured slot widths of 31, 62, 125, and 250 ps. As expected, the error probability increases rapidly when the slot width approaches the combined timing uncertainty of the transmitter and receiver. At $\Delta = 250$ ps, the measured BER is on the order of 10^{-5} , indicating clear separation between adjacent pulse positions. Reducing the slot width to 125 ps increases the BER to the order of 10^{-2} , while further reduction to 62 and 31 ps results in a substantially larger probability of assigning a received pulse to an adjacent slot. The experiment intentionally excludes coding gain in order to characterize the intrinsic timing performance of the modem hardware and the basic PPM demodulator. In particular, neither Gray mapping nor forward error correction (FEC) was applied. The measured dependence therefore directly reflects the combined effects of residual DTC non-linearity, transmitter jitter, receiver timing uncertainty, and remaining synchronization errors after calibration. The 31 ps point is of particular interest because this slot width was configured directly in the Prototype rather than obtained by interpolation or extrapolation. Although reliable uncoded communication is not achieved at this setting, the result demonstrates that the timing architecture remains operational at slot durations close to the receiver single-shot timing uncertainty. For practical operation at these slot widths, additional timing calibration and error-control coding would be required. Moreover, at the smallest investigated slot widths, the PPM pulse duration is considerably longer than a single slot. Consequently, one physical pulse may occupy several adjacent slots; however, symbol information is determined by the position of its leading edge rather than by the pulse duration.

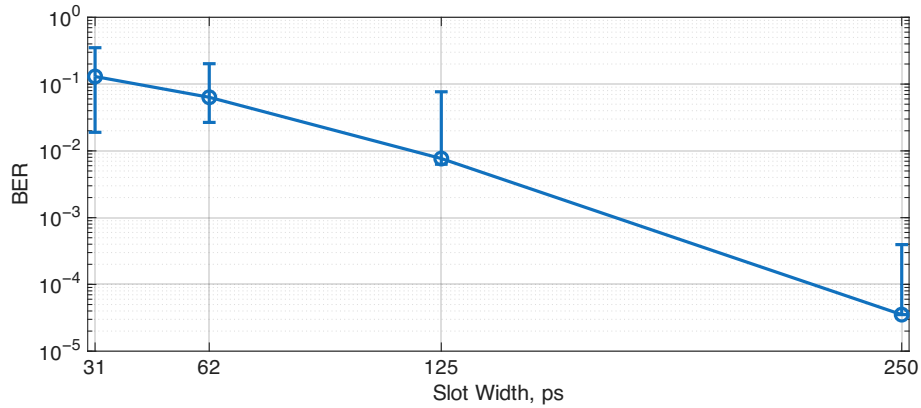


Figure 5. BER of 256-PPM transmission as a function of configured slot width. Each point corresponds to transmission of 313 frames with 16k symbols (in total 1×10^7 bits) using a common 10 MHz reference clock, without Gray coding and FEC.

5. EVOLUTION OF THE PROTOTYPE TOWARD THE ENGINEERING MODEL

The TRL4 Prototype presented in this paper represents an intermediate and still unfinished stage of the HPE-GSM development. The results reported in Section 4 primarily validate the timing architecture, high-rate PPM generation and reception, calibration, and basic demodulation. Further development of the Prototype will focus on implementation of a CCSDS-oriented communication chain, including SCPPM, synchronization, and FEC. Only after these functions have been implemented and validated will the activity proceed to development of the TRL5 Engineering Model.

5.1 Integration with Free Space Optics

In parallel with completion of the Prototype modem, a bidirectional PPM-compatible FSO subsystem is being developed for operation in the optical C-band, approximately 1530–1567 nm. Dedicated transmitter and receiver front ends interface the electrical PPM signals with a laser source and a high-speed photodetector. Because the information is encoded in pulse arrival time, the optical subsystem must preserve the timing characteristics of the waveform while introducing sufficiently low additional jitter. Initial integration will use a laboratory-scale optical link to validate compatibility between the modem and the optical front ends.

5.2 Engineering Model

After completion and validation of the Prototype, the modem architecture will be transferred to a TRL5 Engineering Model. The EM will integrate the modem electronics and an embedded host computer into a self-contained unit with Gigabit Ethernet connectivity. A higher-performance FPGA will be used to migrate time-critical functions, including PPM mapping and demapping, synchronization, interleaving, and coding-related processing, from host-side software to hardware.

The EM is intended to support operation compatible with CCSDS 141.0-B-1 and 142.0-B-1 while retaining custom high-rate modes. The project targets approximately 300 Mbit/s for the fully CCSDS-compatible configuration and up to 800 Mbit/s for custom operation. The EM will incorporate an optical C-band FSO subsystem from Astrolight,¹⁴ including optical amplification and PAT functionality. Final validation is foreseen using bidirectional User Datagram Protocol over Internet Protocol (UDP/IP) data transmission over a kilometre-scale ground FSO link.

6. CONCLUSION

This paper presented the preliminary development and experimental evaluation of the HPE-GSM ground-segment PPM modem based on TDC and DTC techniques. The current TRL4 Prototype represents a transition from the earlier time-tagger-based architecture toward a dedicated integrated modem with substantially reduced receiver dead time, configurable modulation parameters, and integrated calibration and data acquisition. Experimental measurements confirmed operation with slot widths down to 31 ps. For 256-PPM, the measured uncoded BER showed a strong dependence on slot width, with increasing error probability as the slot width approached the combined transmitter and receiver timing uncertainty.

The Prototype presented here is still under development and does not yet provide the complete functionality foreseen for the activity. The next stage will extend the Prototype with SCPPM, synchronization, and FEC functions required for closer alignment with CCSDS 141.0-B-1 and 142.0-B-1. After these functions have been implemented and validated, development will proceed toward the TRL5 Engineering Model, integrating higher-performance real-time processing, standard network interfaces, and the C-band FSO subsystem.

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