

Enhancing Satellite Data Capacity through High-Speed Serial Optical Links on the OneSat Platform

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ABSTRACT

The acceleration of global demand for high-throughput satellite (HTS) communication and high-resolution Earth observation pushed for continuous innovation and development in the satellite payload design. Modern satellites' payload platforms, such as recent development of the flexible Airbus Defence and Space OneSat platform, require a massive on-board processing capability to support advanced payload solutions like dynamic beamforming, large user capacity and sophisticated signal routing. However, maximizing the data throughput is often limited by the physical constraints of the traditional electrical interconnects. The integration of high-speed serial optical transceivers and fiber optical links with the next generation Hyperion Digital Processor on the OneSat platform demonstrates a significant increase in payload data capacity and efficiency. This transition results in a considerable reduction in the traditional satellite harness mass and volume yielding critical savings in launch costs. In addition, the optical links offer an intrinsic immunity to electromagnetic interference and electrical isolation which simplifies the system level design and ensures a robust and error-free data transmission in the electrical dense satellite environment. This paper will present the implementation of high-speed serial optical links in the Hyperion Digital processor, a core component of the OneSat platform for next-generation HTS applications. It will provide a trade-off of this optical solution with traditional electrical technology, evaluating its benefits in Size, Weight, and Power (SWaP). The paper will also examine payload challenges, specifically maintaining satellite capacity despite optical link failures, and will conclude by discussing the future of intra-satellite optical links, focusing on data rate speed beyond 28 Gbps.

Keywords: Satcom, high-throughput satellite (HTS), On-board Digital Processor (OBP), High Speed Serial Links (HSSL), Size-Weight and Power (SWaP), Digital Intra-Satellite Optical Interconnect.

1. INTRODUCTION

In the evolving of high-speed communication and ubiquitous broadband access, telecommunication services must adapt to support high-capacity user demands, including broadcasting, mobile communications, and high-definition video streaming. These requirements necessitate that telecom satellite manufacturers progressively implement advanced technologies and adapted solutions to mitigate data capacity bottlenecks, thereby providing more flexible and economically competitive solutions across all frequency bands and service types.

Conventional Geostationary (GEO) satellites are typically engineered for specific missions with fixed designs and high upfront capital expenditure. Their static resource allocation, where capacity is trapped in specific beams, presents significant risk if the initial design is misaligned with market needs, and their lifecycle value depreciates as market demands shift over time. In contrast, Airbus Defence and Space has introduced OneSat, a software-defined platform that minimizes this risk. OneSat allows for dynamic, real-time resource allocation and reconfigurable beams, ensuring capacity follows demand. While this approach involves higher initial complexity, it offers a superior long-term return on investment, as the satellite's value increases through in-orbit software updates that adapt to evolving market requirements, allowing a single platform to serve needs that would otherwise require multiple traditional satellites.

OneSat allows operators to reconfigure the satellite's capacity (bandwidth, power, and beam shape) via software while it is already in orbit, enabling the spacecraft to adapt seamlessly to changing market demands, such as dynamically shifting capacity from a quiet ocean area to a busy urban area. OneSat operates with the latest advanced digital on-board processor, Hyperion, a critical component of the Airbus OneSat platform designed for next-generation High Throughput Satellite (HTS) applications. Within this processor, all digital signal routing,

switching, and beamforming are performed entirely in orbit, allowing for full flexibility, frequency rearrangement, and dynamic capacity reallocation.

To support these massive data streams, the Hyperion processor relies on digital high-speed serial links (HSSLs) based on optical transceivers and a central fiber flex shuffle network that carries all digital data and control signals between individual ASIC modules [1-3]. This transition to optical fiber links significantly outperforms traditional electrical interconnect links, which are limited in bandwidth, suffer from high insertion loss, and present severe challenges regarding signal integrity. Traditional electrical backplanes also require an impractical number of stack layers to handle high data rates. In contrast, the integration of fiber optics provides intrinsic immunity to electromagnetic interference (EMI/EMC) and complete electrical isolation, ensuring robust and error-free data transmission within the electrically dense satellite environment. Furthermore, this advanced photonics solution substantially reduces traditional satellite harness mass and volume, yielding critical savings in both payload space and overall launch costs.

This paper presents the implementation of high-speed serial optical links within the Hyperion Digital processor, covering the design of optical transceivers, the high-density fiber harness architecture, and the comprehensive space environmental qualification campaign. It evaluates the benefits of this photonic solution regarding Size, Weight, and Power (SWaP) and signal integrity, and provides a future insight on the next-generation of the intra-satellite optical interconnects, including the potential of co-packaged optics.

2. DIGITAL ON-BOARD PROCESSING HERITAGE

Airbus Space and Defence has a long heritage in developing and delivering digital on-board processing solutions going back to the 1990's. Airbus's space payload processing capabilities have evolved significantly across five generations. The trajectory spans early analog-conversion systems to fully software-defined, direct-RF sampling payload processors. Across these generations, Airbus has prioritized increasing bandwidth, modularity, connectivity, and onboard computing power while achieving drastic reductions in Size, Weight, and Power (SWaP) and cost-per-Gbps.

The 1st generation of the on-board processor was developed with the support of the European Space Agency (ESA) for delivery to the Inmarsat 4 series of spacecraft, allowing for flexible channelization and routing of signals. The processor itself had to solve many of the issues we still see today; high power dissipation and mass along with highly integrated and never before flown technology, whether that be Application Specific Integrated Circuits (ASICs), Multi-Chip Modules (MCMs), Analog to Digital Converter (ADC) / Digital to Analog Converter (DAC), etc.

The 3rd generation of on-board processor (NGP) was again developed with the support of ESA, but targeted for the first time to serve more than once mission type, Narrowband, Broadband, Digital Beamforming, integrated RF, on-board calibration and a high-speed link for telecommand and telemetry. Compared to the 1st generation, the new processor extended the processed spectrum for mobile communications and increased the signal dynamic range capability by 10 dB. It also incorporated for the first time a built-in self-calibration system to support the phase tracking needed for accurate digital beam-forming without constraining the use of the latest digital technologies.

The 4th generation on-board processor (SMP) was originally developed to extend the broadband capabilities of the Gen3 processor, i.e. increase the maximum possible bandwidth per port and also the maximum processor capacity with and without digital beamforming. Higher frequencies are supported at the signal interfaces to simplify the analogue pre- and post- processing. More capable ASIC processing technology also greatly extends the signal dynamic range supported per channel. The 4th generation processor is more flexible than either Gen 1 or Gen3 because it has full user-to-user (and gateway-to-gateway) connectivity.

On board-processing Gen 5 or Hyperion is the latest development processor and is the main concept for a fully flexible satellite in OneSat platform. Hyperion capability can enable adaptation to several types of mission. The processor has fully functional integrated architecture where there is no pre- or post-processor external to DTP. The digital beamforming and switching are carried inside the DTP module with frequency up to Ka-band. Mass

and power consumption per gigabit have dropped dramatically, enabling flexible multi-beam payloads to fly on smaller, cost-effective satellite platforms. The Hyperion process allow for I/O port up to 3 GHz, and capacity of several 100 GHz.

3. HYPERION PROCESSOR CONFIGURATION

Hyperion processor handles massive digital signal routing, beam-forming, and dynamic spectrum allocation entirely in orbit. This processor is made of by far the most complex application specific integrated circuit (ASIC) undertaken by space systems, which carries out almost all the active traffic processing on the Airbus OneSat satellite. The efficient use of spectral resources and phase array elements implies multibeam satellite coverage associated digital beamforming and routing flexibility between beams. The complete Hyperion Processor is composed of three boxes as shown in Fig.1 which can be distributed across the payload system. Each box contains a set of modules for receive, transmit, switching, and control signals. The processor modules are fully interconnected using optical high speed serial links to transfer digital data and control signals.

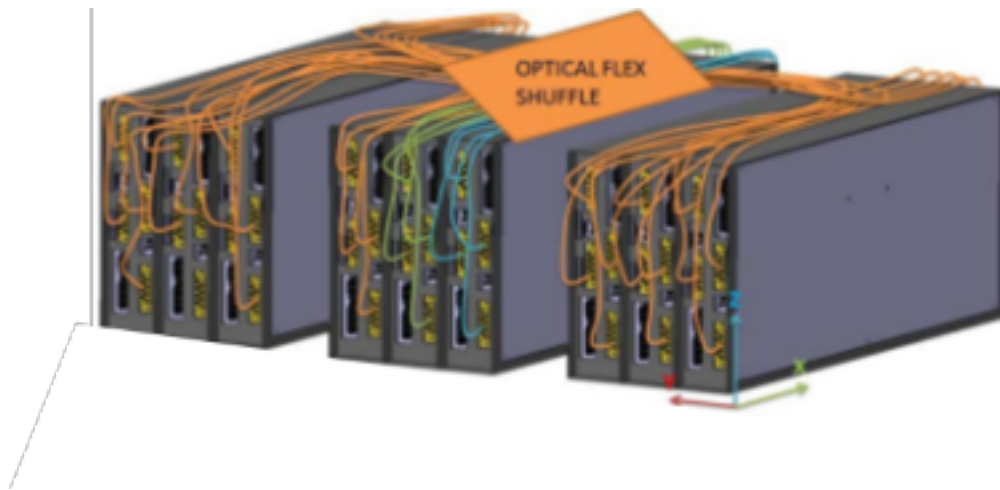


Figure 1. Hyperion DTP processors with central fiber optic interconnect on central DTP

The DTP processors directly interface with a large number of receive and transmit RF phased array antennas with two polarizations and more than 3 GHz bandwidth. The RF signals are digitalized and channelized into sub-channels. The optical links transfer between the digitized signals between modules. The high-speed serial link between the ASICs is based on the optical modules using 28G 12-channel transmit and receive opto-electrical devices, interconnected by a high-density optical fiber network. The digitized sub-channels can be digitally beamformed and routed allowing for frequency rearrangement, and capacity reallocation. These sub-channels are recombined, routed and beam-weighted sub-channels into broad downlink spectrum bands. The wideband digital stream passes through high-performance DACs, converting the processed digital words back into continuous analog RF signals. Fig. 2 shows the Hyperion processors with optical fiber links interconnecting between the ASIC modules.

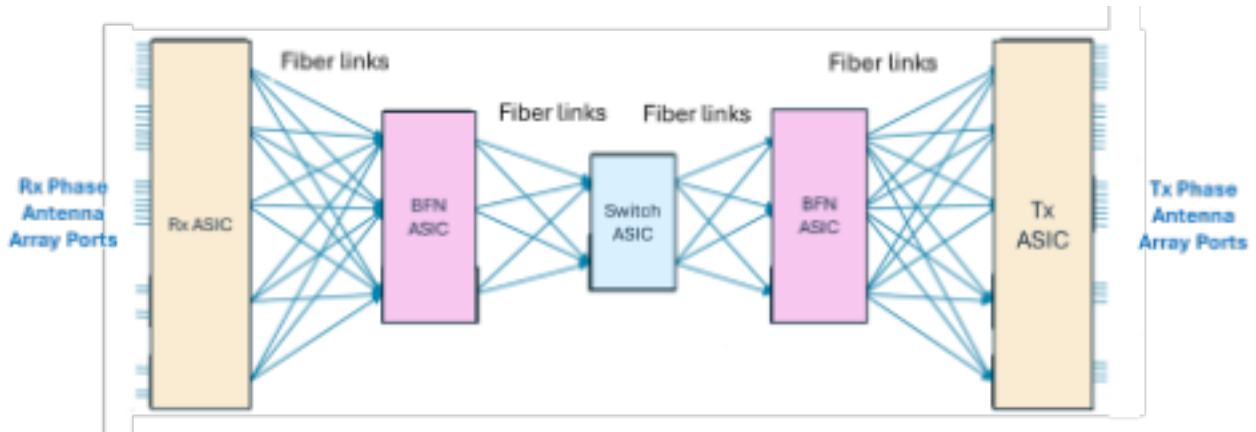


Figure 2. Hyperion Digital Processor architecture and high-speed serial optical link interconnectivity.

4. DIGITAL OPTICAL TRANSMIT AND RECEIVER MODULES

The optical links interconnecting the ASICs serve as the core communication components for the Hyperion/Gen5 architecture, utilizing high-density optical modules to facilitate multi-channel connectivity. The development and space environmental qualification of these digital optical transmitter and receiver components, including the high-density optical harness, were successfully achieved under the ESA-funded ARTES Scylight program. The active opto-electronic parts were meticulously selected to satisfy the rigorous performance and capacity requirements of the on-board digital processor. These requirements establish a baseline configuration consisting of a 12-channel half-duplex optical transmitter (12Tx) and receiver (12Rx) integrated into a compact, ruggedized package (shown in Fig. 3). Each channel operates at a baseline data rate of 28 Gbps in an NRZ encoding format, supporting a robust end-to-end link budget. The optical transmitter utilizes a multimode 850 nm directly modulated Vertical-Cavity Surface-Emitting Laser (VCSEL) device. The optical receiver uses high speed GaAs PIN photodiode.

To ensure ease of volume manufacture, the optical module is mounted onto the host PCB using a solderless LGA interposer. Although implementing this interposer version did require overcoming design challenges, it uniquely enables the replacement of optical transceivers directly within the satellite payload. The optical interfaces are based on multimode fiber with a 12 MT optical connector. The optical interface at the 12TX or 12RX chips will be based on MT ferrules as these allow for high density fiber connections. The optical 12TX or 12RX chips will be placed as close as possible to the corresponding ASIC in order to help with the signal integrity and also reduce the SerDes power dissipation.



Parameters	Value
Optical Device	VCSEL / PIN GaAs
No. Channels	12Tx or 12Rx
Bitrate	28 Gbps
Modulation	NRZ
Operating Wavelength	850 nm
Power Consumption	Less than 6W for 12 links
Optical Interface	12 MT

Figure 3. Representative of the optical Tx/Rx device and their specifications

The environmental qualification of Tx/Rx modules was tailored to exceed the device standard stress levels. The following table (Table 1) summarizes the qualification test campaign for the optical transmit and receive parts. The 12TX/12RX parts were first evaluated and functional verified in the first Hyperion engineering model (EM1). Secondly, the suppliers conducted design verification test (DVT) campaigns including acceptance tests over temperature and EMI tests. These components have been fully validated to survive a space environment lifetime of at least 15 years. Following the successful completion of the DVT campaigns, the suppliers conducted the qualification test programme (QTP) which were in agreement with Airbus specifications. This included an environment test programme of the latest version of the RX and TX devices with interposers comprising vibration, shock and thermal cycling compliant to the Hyperion mechanical requirements. In the mechanical qualification, the devices successfully withstood severe stress levels reaching up to 60 Grms, which required close engineering coordination with the supplier to customize the chassis and fully satisfy the platform's mechanical constraints. Finally, Airbus completed the advanced PCB engineering models and the internal qualification activities. A comprehensive performance validation is conducted by monitoring critical parameters such as Bit Error Rate (BER) measurements, continuity resistance, and Received Signal Strength Indicator (RSSI) levels. During testing, minor variations in the analogue telemetry (TM) for RSSI and IBIAS were observed; however, these are recognized characteristics of the optical transceivers and have been accepted as operational anomalies that do not threaten performance link integrity. Structural testing revealed that mechanical vibration levels were highly amplified by the large host PCB board, necessitating structural modifications to the chassis.

Table 1. Qualification test campaign for optical devices.

Test ID	Qualification Test	Standard / Method
1	Radiation	Heavy ions: ESCC 25100 Iss. 2; TNID: 100MeV protons; TID: ESCC 22900 Iss. 5 (Gamma rays Co ⁶⁰).
2	Outgassing	ECSS-Q-ST-70-02C; RML < 1.00%, CVCM < 0.10%.
3	Rapid Decompression	MIL-STD-810G, Method 500.5, Test Condition III.
4	Vibration	28+ Grms
5	Mechanical Shock	1500g 0.5ms.
6	TVAC	-40°C to +85°C; 20 cycles; 5x10 ⁻⁵ mbar; Monitored;
7	Thermal Cycling	-40°C to +85°C; 1,000 cycles.
8	Damp Heat	85°C / 85% RH; 500 hrs; post-baking for 68 hrs at 85°C.
9	Life Test	4,000 hrs @ 90°C; Biased test @ 90% max current.

5. OPTICAL FIBER HARNESS NETWORK

The optical interconnection between Hyperion modules is implemented by employing advanced fibre optic flexible routing technology. This technology is based on embedding or printing optical fibers into flexible, ruggedized polymer films designed for internal spacecraft and satellite backplanes, which significantly reduces the mass, volume, and complex wiring constraints traditionally encountered in aerospace payloads. The flex technology effectively supports high-density signal routing, capable of handling hundreds to thousands of parallel optical channels while offering high mechanical durability to withstand intense launch vibrations and thermal shocks. Within the Hyperion digital processor, the optical harness architecture is divided into two primary components: an internal patchcord harness that routes signals inside the Hyperion modules from the high-density optical transmit and receive transceivers to the exterior of the module, and an optical shuffle harness that establishes

connectivity across all Hyperion modules. The external harnesses are securely routed on top of middle DTP box with a multi-layer stack of protective materials, such as Kapton polyamide or flame-retardant Silicon, in a manner analogous to a printed circuit board routing, which is subsequently encapsulated by applying an identical or similar protective layer stack on top. This comprehensive optical fiber harness incorporates over 2,500 optical links, enabling high-density fiber patterns to be systematically routed to and from ribbon MT terminations. To optimize performance under space radiation environments, the external harness utilizes super radiation-hardened OM2 type fibers, whereas the internal harness employs radiation-hardened, bend-insensitive OM4 type fibers. The overall Hyperion interconnection architecture is structured around a large fiber flex routing board supported on top of several modules; this board provides flying leads that are grouped and terminated on the plug side of the bulkhead connectors to interface reliably with each individual module, completing the integrated flex shuffle network.

The qualification strategy for the fiber optic interconnect is split between the fiber optic supplier and Airbus to ensure rigorous spaceflight validation. The qualification programme is systematically organized into five distinct test groups. Groups A and B are executed entirely by the fiber optic supplier, focusing primarily on the bulkhead connectors and covering critical environmental and mechanical tests such as temperature cycling, damp heat exposure, tensile strength, torsion resistance, mate/demate durability, vibration, and shock testing. Group C is conducted by Airbus as an integral part of the Hyperion engineering qualification model validation, where the complete end-to-end, flight-representative optical chain is subjected to thermal vacuum cycling, vibration, and shock to verify system-level performance. Group D encompasses a high-temperature survival campaign carried out by the fiber optic supplier using a dedicated test vehicle that includes every single component within the interconnect chain. Finally, Group E consists of specialized radiation test campaigns led by the fiber manufacturer to validate the radiation tolerance and long-term reliability of the two types of optical fibers employed throughout the Hyperion optical assemblies.

The development and implementation of the optical harness were subject to various technical challenges and manufacturing difficulties. Fiber handling is inherently delicate and requires meticulous care during carrying, packaging, and installation phases, as any fiber breakages or misrouting could cause severe degradation to the payload performance. Additionally, contamination of the fiber end-faces during polishing and cleansing operations represents a critical issue that directly affects Insertion Loss (IL) and Return Loss (RL), potentially causing complete loss of connection during initial orbital operations or over the spacecraft's operational lifetime. Fiber bending radius constraints also impose structural limitations on the fiber assemblies. Given the large number of required fiber assemblies, managing these constraints significantly increases the complexity and time required for routing, testing, and verifying the fiber paths. Furthermore, performing repairs or fusion splicing presents extreme difficulty if damage or anomalies occur internally within the flexible routing layer or in close proximity to it. Moreover, rigorous cleaning and inspection of fiber end-faces are essential to prevent contamination and foreign object debris (FOD), which are primary causes of performance degradation and can lead to intermittent or catastrophic link failure.

Despite all of these challenges the optical fiber harness is a competitive solution to the electrical-based interconnections providing flexibility of the system, no EMI/EMC impact and the whole system can benefit from low mass and size performance. Traditional electrical interconnects, such as SpaceWire or CAN bus, have long served as reliable standards for lower-bandwidth control and telemetry. Table 2 shows the trade-off performance between traditional SpaceWire versus Optical HSSL. The copper-based solutions encounter significant physical and performance bottlenecks. The SpaceWire speed is capped at 200Mbps, compared to 140 times in a single fiber lane. The SpaceWire's signal suffers from cross talk and degradation where the fiber link is totally immune to EMI and low losses. In addition, the optical interconnects deliver superior size and power metrics where their size is 2.3 less than SpaceWire, and 17 times lower mass density.

Table 2: Comparative Performance Metrics: Traditional SpaceWire vs. Optical HSSL

Feature	SpaceWire	Optical HSSL	Benefit Ratio (Optical/SpW)
Links per Cable	2	12 to 24	6x - 12x

Feature	SpaceWire	Optical HSSL	Benefit Ratio (Optical/SpW)
Mass Density	40 - 85 g/m	5 - 20 g/m	2x - 17x Reduction
Cable Diameter	7 mm	3 mm	~2.3x Reduction
Data Rate (per lane)	Up to 200 Mbps	Up to 28 Gbps	~140x Increase
EMI/EMC Immunity	Low (Shielding Req.)	Intrinsic (Dielectric)	High
Electrical Isolation	Required (Galvanic)	Inherently Isolated	Full

6. OPTICAL LINK PERFORMANCE

The performance of the Hyperion high-speed serial optical links is verified through a rigorous validation strategy that combines system-level link budget analysis with comprehensive hardware qualification. Ensuring robust connectivity over a 15-year mission lifetime requires maintaining a Bit Error Rate (BER) of less than 10^{-9} , a target achieved through a conservative end-of-life (EOL) optical link budget. This budget accounts for several degradation factors, including thermal effects, and aging on laser output, radiation-induced attenuation (RIA) in the fiber, and insertion loss (IL) across multiple optical interfaces.

Validation of the end-to-end optical chain is conducted by monitoring critical parameters, specifically Received Signal Strength Indicator (RSSI) levels, continuity resistance, and real-time BER performance. During initial verification, minor variations in analogue telemetry for RSSI were observed; however, these have been characterized as operational behaviors inherent to the transceiver design and do not compromise link integrity.

The qualification campaign highlighted several critical design challenges, particularly regarding mechanical stress. Early structural testing revealed that mechanical vibration levels were significantly amplified by the large host PCB backplane, necessitating structural modifications to the module chassis to achieve compliance with the 60 Grms requirement. Additionally, the sensitivity of the optical interconnects to end-face contamination—a known driver of Insertion Loss (IL) and Return Loss (RL) degradation—required the implementation of stringent cleaning and inspection protocols throughout the assembly and integration phases.

Furthermore, environmental testing confirmed the resilience of the selected fiber types. By employing super radiation-hardened OM2 fibers for external harnesses and bend-insensitive, radiation-hardened OM4 fibers for internal routing, the system maintains performance stability despite the harsh ionizing radiation and thermal cycling environments encountered in orbit. This multi-faceted validation approach confirms that the optical links are fully capable of supporting the high-throughput, dynamic routing requirements of the OneSat platform.

The optical HSSLs serve as the primary interconnects between ASIC modules. A failure in one of these links could lead to a reduction in processing capacity, potentially jeopardizing mission operations. Leveraging the software-defined payload architecture, the reconfigurable processor can mitigate this risk by rerouting bandwidth and signals to alternative operational or redundant links.

7. FUTURE OF INTRA-SATELLITE OPTICAL INTERCONNECTS

Intra-satellite optical links are expected to have high growth in the next generation of the satellite payloads because modern high-throughput satellites process massive streams of communication data. In the modern satellite process, the high RF frequency and multi-beamforming push the aggregated data rate to reach from several of 100 Gbps to over 1Tbps resulting from the increase of the phase antenna arrays. Due to a large number of phase antenna elements, it would be required to form, steer, and dynamically change multiple beams at the same time; every signal element must be individually controlled with precise digital data. In addition to this, the ADC/DAC sampling for radio- signals at ultra-high frequencies would require an increase of the raw data per second making the internal data routing requirement instantly skyrocket into the Terabits-per-second range.

To accommodate the future global bandwidth demands and large phase array antennas, the technology roadmap targets scalability beyond 25 Gbps up to 56 Gbps and 112 Gbps high-speed optical links, leveraging mid-board transceivers and co-packaged optics directly integrated with the ASIC [4]. As data rates increase, the electrical paths between optical transceivers and SerDes become the main source of signal degradation. The longer trace lengths introduce signal loss, requiring high performance DSP/SerDes and more power consumption significantly at higher speeds. Therefore, moving optical transceivers closer to the ASIC reduces electrical trace lengths, which minimizes high-frequency signal loss, lowers power-hungry SerDes and DSP requirements, and prevents the system from hitting the severe energy limits of the "I/O power wall". Co-packaged Optics (CPO) is a transition shift by integrating the optical engine closer to the ASIC package, minimizing the electrical path from centimeters scale to millimeter scale and dramatically reducing signal loss achieving power consumption of lower than 5pJ/bit. This matches exactly with the requirements of the SWAP of the future digital payload.

There are challenges to deploy the CPO transceivers into the space environment. It would be required to overcome space environmental hurdles. The silicon photonic devices have to become evaluated in the rad-hard design feature. Thermal management is becoming the main issue to maintain the required temperature as it is included in dense areas. The devices have to survive the initial vibration and shock. The strict outgassing rule and the remote laser architecture laser diode cannot be embedded next to the processor; they are isolated in separate shielded external modules.

8. CONCLUSIONS

The transition from traditional electrical interconnects to high-speed serial optical links within the Hyperion Digital processor marks a transformative shift in satellite payload design. By integrating advanced optical transceivers and high-density fiber harnesses, the OneSat platform achieves a significant increase in data capacity while simultaneously realizing critical reductions in harness mass and volume. Furthermore, these optical links provide intrinsic immunity to electromagnetic interference and superior electrical isolation, ensuring robust signal integrity in the dense electrical environment of modern satellites. The successful space qualification and implementation of these modules demonstrate their reliability and essential role in enabling the full flexibility and high-throughput performance of software-defined satellite missions.

Looking ahead, the scalability of optical technology remains the primary pathway for meeting the burgeoning global demand for multi-Terabit-per-second capacity. The roadmap toward co-packaged optics (CPO) and data rates exceeding 28 Gbps aims to overcome the "I/O power wall" by drastically shortening electrical paths and reducing signal loss. While engineering challenges such as precise thermal management, radiation hardening of silicon photonics, and surviving the harsh mechanical rigors of launch persist, the continued advancement of intra-satellite optical links remains fundamental to realizing the next generation of high-throughput, software-defined satellite missions.

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