

Bit-Stream Recorder and Modem for Optical On-Off-Keying Satellite Downlinks

Dirk Giggenbach^a, Florian Lippert^a, Nibedita Chakraborty^b, Anusha Bhandari^b, Oliver Lücke^b,
Muhammad Asad^b, Mojtaba Najafi^b, Marcus T. Knopp^c

^aInstitute of Communications and Navigation (IKN), German Aerospace Center (DLR),
82234 Oberpfaffenhofen, Germany

^baeroLiFi GmbH, 82234 Wessling, Germany

^cResponsive Space Cluster Competence Center (RSC³), German Aerospace Center (DLR),
82234 Oberpfaffenhofen, Germany

ABSTRACT

Optical Data Downlinks from Satellites are becoming the standard in high-speed space networks of LEO (low Earth orbit) mega-constellation systems for commercial use, in repatriation of Earth observation data from LEO, or for military use. Benefits are a vast increase in data rate, the size-, weight-, and power-advantages, and the inherent security of directed free-space optical communications (FSO), in contrast to conventional RF communications. The basic choice of modulation format in Optical LEO data downlinks (OLEODL) for links through the distorting atmosphere is optical on-off-keying (OOK), while also complex modulation formats will be used in other application scenarios. We show a viable solution for the data stream reception and processing of various transmission standards.

1. INTRODUCTION

For the basic use of optical satellite downlinks, the incoherent OOK format [1] has been standardized by the Consultative Committee of Space Data Systems (CCSDS) in so called Blue Books [2] and [3], suggesting data rates of 10Gbps and fractions below. Furthermore, the Space Development Agency (SDA) released a similar standard document [4] with data rates of 2.5Gbps and below. A basic characteristic of the standards is the huge range of potential data rates, combined with a selection of FEC rates and interleaving concepts, to cope with

- strong variations in distance (and thus in free-space loss) [5]
- different system component properties like Rx-aperture sizes and Tx-divergence angles (stemming from the space terminal's achievable pointing precision) [6]
- varying meteorological conditions (Index-of-refraction turbulence and attenuation) [8][9][10]

Existing space-terminal hardware is currently used for the evaluation of both standards mentioned above, where several optical ground stations (OGS) serve as counterparts [11][12]. Highspeed data reception poses a new challenge to backend receivers/MODEMS at the ground stations, where data rates hitherto have been limited to below some hundreds of Mbps in conventional RF downlinks. For optical technology, costly electronics now has to be used to cope with the processing of much higher data rates, mostly based on Field-Programmable Gate Array (FPGA) technology.

Here we want to circumvent the need for a new development for each communication layout, by assuring the unrestricted high-speed reception of the serial data, by means of a **Bit Stream Recorder (BSR)**, while providing the subsequent data processing by conventional software algorithms running on CPUs. This enables to avoid the detailed implementation of a communication standard, but only those basic features necessary for reception of the high-speed serial data in a specific mission or terminal type. Through this, we achieve a significant reduction of complexity and, hence, costs, on the sheer high-speed OGS receiver electronics, which allows to focus expenses on other relevant OLEODL technology parts. We show and discuss how such an approach supports flexible wide-spread test and verification missions for different optical standards and payloads, as well as providing a persistent cost-efficient method for all non-real-time communications.

2. TRANSMISSION SYSTEM OF OLEODL

The typical OLEODL scenario is illustrated in figure 1: When the satellite appears above the horizon at typically 5° to 10° elevation, the OGS starts illuminating the satellite with its beacons (based on its orbital knowledge) to support the satellite's pointing algorithm. As soon as the satellite starts to track the OGS beacons, it switches on the data signal. When the satellite again reaches low elevations, the data signal experiences maximum distortion and is finally cut off, terminating the downlink.

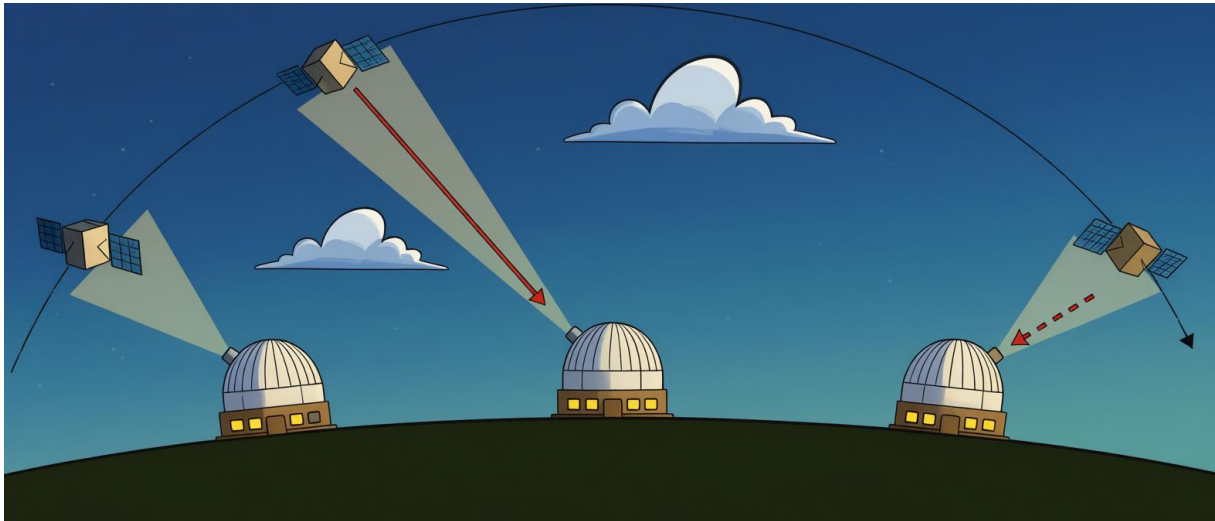


Fig 1: The Optical LEO Downlink Scenario (adapted from [6])

The processing chain of the OLEODL scenario is shown in detail in figure 2. The free-space channel introduces perturbations on the satellite's laser signal through atmospheric attenuation, distance variation and wavefront distortion caused by index-of-refraction turbulence (IRT). Received and amplified by the telescope, the optical signal is split into two paths - the concept of such a system is explained in [13]. An IR camera is feeding back into the telescope mount controller to enable tracking of the moving target. The main part of the signal is received by the data detector where often high-sensitivity APD-based (avalanche photodiode) receiver frontends (RFE) are used [14][15]. The RFE converts incident optical power into a differential electric signal feeding into the modem. The modem can provide digital data processing of various kinds before transmitting payload data to some kind of network storage or for immediate use in a communication scenario.

For the uplink signal, a laser source is used which should be modulated with a pulsed beacon signal to enable masking distortions from background light. Or it can even be used for data transmission or telecommand (indicated in fig. 2 by the dashed arrow from the right). The uplink transmit telescope is mechanically connected to the receiving telescope. After leaving the transmit aperture, the free-space

channel perturbrates the uplink signal once again before it reaches the satellite. However, the uplink channel model differs significantly from the downlink channel [16].

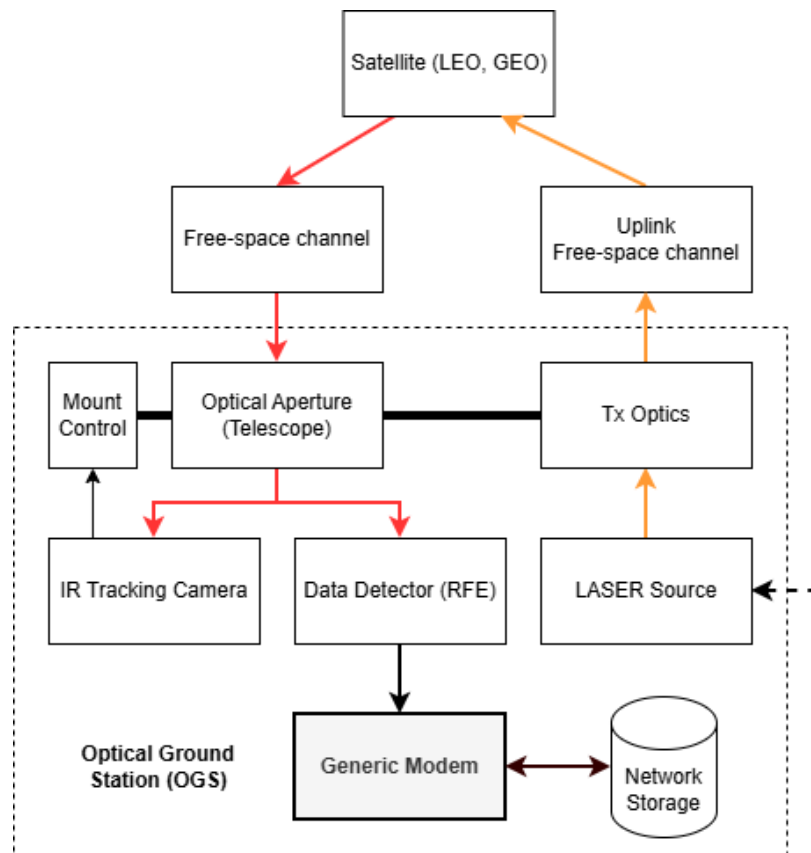


Fig 2: Data processing chain in an Optical LEO Satellite Downlink

3. DATA-FORMATS FOR THE O3K LEO-DOWNLINK

The primary advantages of adopting standardized communication protocols are their robust interoperability enabling reliable cross-agency communication, and its widespread use across the space industry. These standards define the frame structure, synchronization patterns, coding schemes, error-correction mechanisms, and protocol layers. In this paper, two standards for optical transmission are discussed.

3.1 The O3K-standard of the Consultative Committee for Space Data Systems (CCSDS)

CCSDS foundational signal waveform standards are traditionally adopted by major space agencies (e.g. by ESA, NASA, DLR, and JAXA). This section focuses specifically on the CCSDS 141.0-B and 142.0-B Blue Books framework [2][3], which specifies the data flow of physical layer, and coding- and synchronization-layer.

At the higher-level data link layer, the data is organized into fixed-length transfer frames. The transfer frames can be e.g. Telemetry (TM), Advanced Orbiting Systems (AOS), or Unified Space Link Protocol (USLP) frames. The complete transmission process flow for the frames is illustrated in Figure 3.

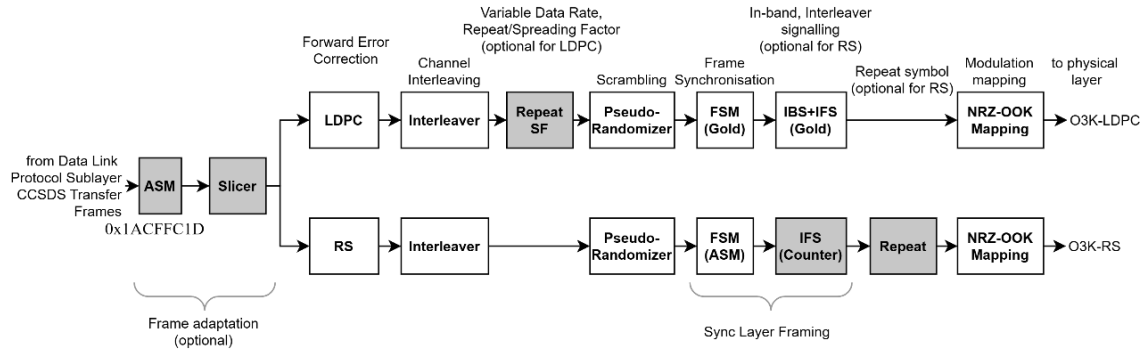


Figure 3: CCSDS processing chain for O3K-LDP and O3K-RS signaling (after [3]).

If transfer frame adaption is used, an Attached Sync Marker (ASM) with hexadecimal value 0x1ACFFC1D is prepended to each transfer frame for frame synchronization, resulting in Synchronized-Marker Transfer Frames (SMTF), which may then be sliced into information blocks of a length compatible with the chosen code type and code rate. The information blocks are then Forward Error Correction (FEC) encoded, either using Low-Density Parity-Check (LDPC) or Reed-Solomon (RS) codes, followed by channel interleaving and pseudo-randomization.

In O3K telemetry signaling, an additional synchronization layer is introduced to structure the transmitted data into Major Code Frames and Subframes. A Sync Layer Frame Marker (SLFM) is prepended to the encoded frame. SLFM comprises a Frame Synchronization Marker (FSM), which is not encoded. The structure of FSM depends on the coding scheme: for RS coding, the FSM is the same as the ASM, whereas for LDPC, the FSM is a Gold-sequence-based 2048-bit pattern. The selected coding scheme determines the additional synchronization steps required. For Low-Density Parity-Check (LDPC) codes, the system employs In-band Synchronization (IBS) and Interleaving Frame Synchronization (IFS) blocks. For Reed-Solomon (RS) codes, the IFS counter is utilized. Prior to transmitting the encoded bitstream, optional symbol repetition may be applied for rate adaptation when RS coding is used.

The CCSDS O3K SLFRAME format can be adapted to specific needs by choosing either RS or LDPC coding and code rate, and further through the managed parameters, e.g. interleaver configuration, frame length, see Figure 3. Also, a wide range of channel data rates from 10Gbps down to few Mbps is supported [2].

3.2 Space Development Agency (SDA) signal format

SDA (Space Development Agency) is the part of the United States Space Force responsible for developing standards for space-to-space, space-to-air, space-to-maritime, and space-to-ground free-space optical communications. The frame construction is defined by the SDA Optical Communications Terminal (OCT) Standard (specifically Version 4.0.0 [4]). The frame construction of SDA is illustrated in Figure 4

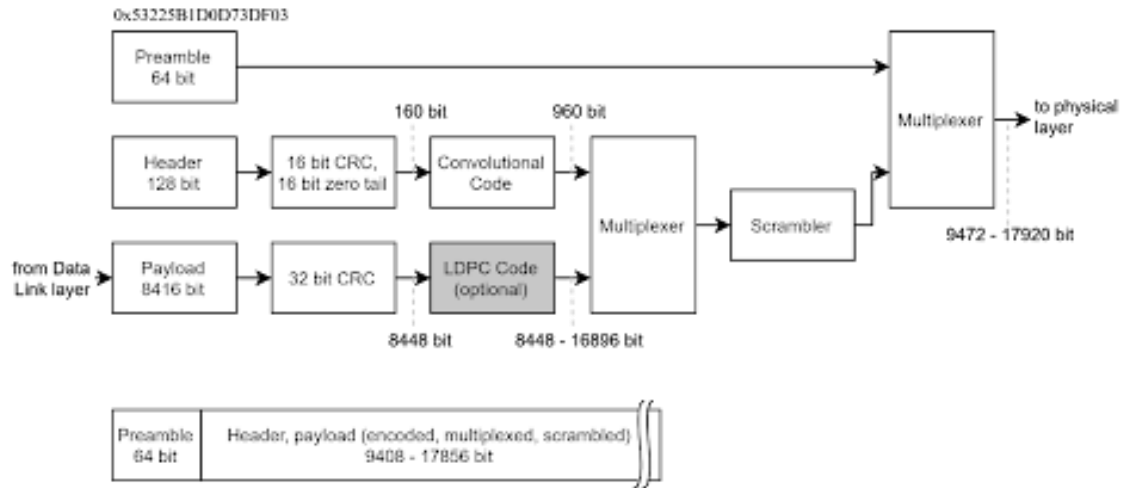


Figure 4: SDA OCT modem frame construction (after [4])

The frame structure of SDA consists of a preamble, a header, and a payload. The preamble is a fixed 64-bit sequence; its hexadecimal value is 0x53225b1d0d73df03. This sequence can be used for synchronization, helping the receiver to detect frames. The header is 128 bits long, it is protected by a 16-bit CRC and a 16-bit zero tail, and then encoded by a Convolutional Code to output a fixed-length 960-bit block. The payload has a length of 8416 bits and is appended with a 32-bit CRC as shown in Figure 3, passing it through an LDPC encoder is optional.

The header and payload are combined in the first multiplexer and then passed through a scrambler. Finally, a second multiplexer appends the preamble to it. The resulting frame length is between 9,472 bits and 17,920 bits. In summary, SDA offers only few potential serial data rates of 2.5Gbps and below, and the frame length varies depending on specific FEC code rate employed.

To receive either data format, a possible modem setup must be implemented (fig. 5). The system consists of an input that receives high-speed serial electrical data, which is fed into a processing platform, typically an FPGA board. The FPGA performs bit-synchronization, frame detection, metadata generation, and buffering, and then forwards the data to the intermediate storage. The recorded data is read out through a LAN interface to a Host PC for software-based processing and analysis.

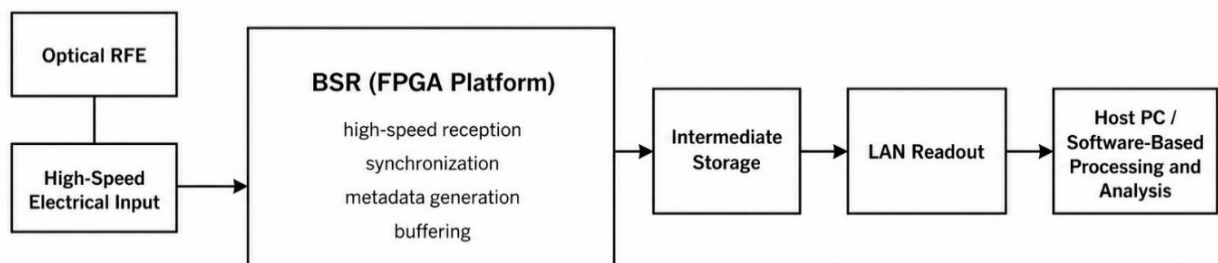


Fig. 5: Generic Modem Implementation

4. THE BIT-STREAM-RECORDER

The motivation to build a BSR is to avoid multiple costly implementations of O3K-modems only to cope with the growing number of experimental and pre-operational optical space-ground link campaigns. The primary objective of such campaigns is to evaluate the link feasibility and reliability rather than to deliver operational mission data. The dominant measurement needs are therefore error-detection and frame-loss determination, which can be met without a complete real-time modem.

The BSR complements rather than replaces such a full-fledged modem. It preserves the received serial stream together with synchronization, integrity and captures metadata, while mission-specific decoding and higher-layer processing are transferred to host software. This separation reduces the protocol-dependent processing that must be implemented in FPGA hardware.

The baseline system boundary begins with the conditioned high-speed electrical signal delivered by the RFE and ends with the recorded bit stream and its associated metadata. Optical detection, analogue receiver calibration, real-time FEC decoding and higher-layer payload processing lies outside the baseline BSR functionality. The BSR targets configurable serial O3K data rates up to 10 Gbit/s, covering the range addressed by the CCSDS non-coherent optical physical-layer and coding-and-synchronization standards [2][3].

The functional architecture of the BSR is shown in fig. 6. The implementation is partitioned between the programmable logic (PL) and the processing system (PS) according to the timing and throughput requirements of the individual functions. The PL contains the real-time Bit-Stream Recorder core and performs the high-speed, deterministic processing directly on the incoming electrical data stream. This includes serial reception, word alignment and rate adaptation, synchronization and marker detection, protocol-pattern recognition, signal-quality assessment and generation of capture metadata. Keeping these functions in the PL enables continuous processing at multi-Gbit/s data rates without interruption by software execution.

The captured stream and its associated metadata are then transferred by Direct Memory Access (DMA) to the PS. The PS manages the DDR buffer memory, intermediate storage and LAN-based host interface, which are less timing-critical and benefit from software control and flexible data handling. The recorded data can subsequently be transferred to a host PC for offline decoding and detailed analysis. This PL/PS partition therefore separates deterministic high-speed acquisition from storage, communication and mission-specific post-processing, allowing the BSR to support CCSDS SLFRAMES, SDA OCT modem frames and configurable test patterns within a common architecture.

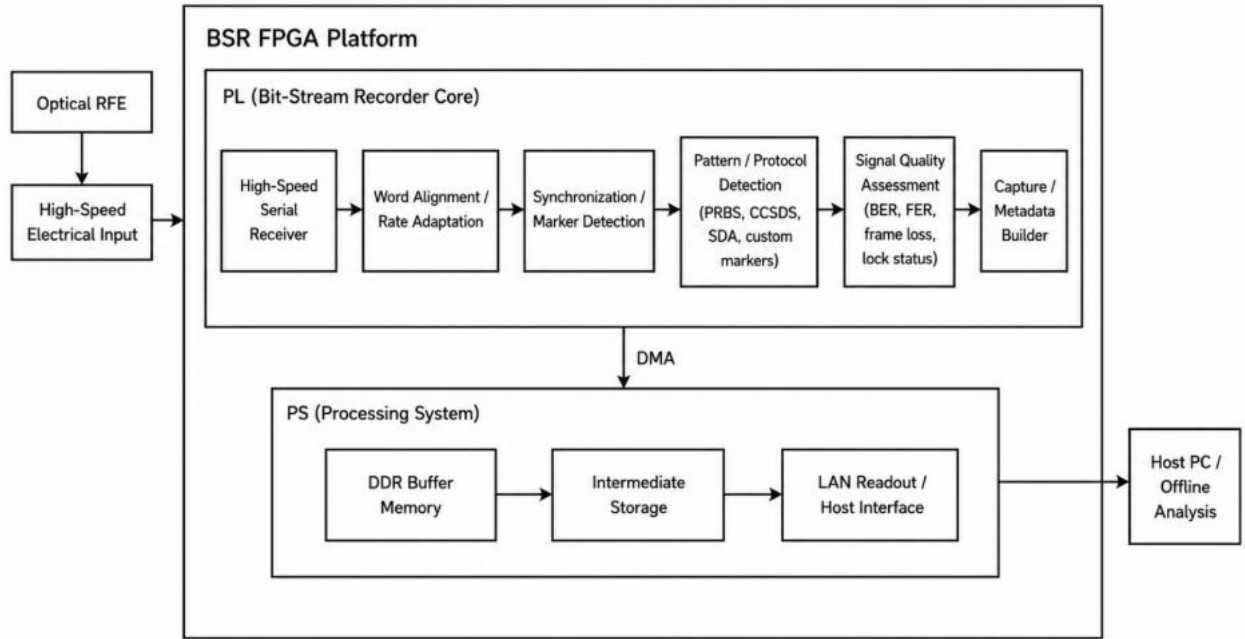


Fig. 6: BSR functional architecture and PL/PS partitioning

For CCSDS reception, frame synchronization is based on the synchronization structures defined for the selected coding mode, including the Attached Sync Marker (ASM) and the corresponding frame synchronization marker [3]. For SDA reception, a fixed 64-bit preamble identifies the start of an OCT modem frame [4].

In addition to detecting and synchronizing to sync-markers, the BSR recognizes further predefined serial patterns so that reference bit streams can be validated, as summarized in Table 1. The supported pattern classes include PRBS sequences, the CCSDS ASM and the SDA preamble, Ethernet preamble, and arbitrary user-defined symbols.

Table 1: BSR detection pattern options

Symbol	Length (Bit)	Pattern / polynomial	Purpose
PRBS	Variable	$x^a + x^b + 1$	Testing and validation
CCSDS ASM	32	0x1ACFFC1D	Frame Synchronization
SDA Preamble	64	0x53225B1D0D73DF03	Frame Synchronization
Ethernet Preamble + SFD	64	0x55555555555555D5	Frame Synchronization
Arbitrary Symbol	User-defined	User-defined	Custom protocols

Fig. 7 summarizes the complete functional chain of the BSR from signal input to software-based post-processing. The optical or electrical input block represents either the output from an APD-based receiver front end or a laboratory test source. The high-speed front end then performs clock recovery, serial-data acquisition and rate adaptation so that the incoming bit stream can be processed reliably at the selected operating rate.

The synchronization and format-detection stage searches the received stream for predefined patterns such as PRBS sequences, Ethernet preambles, CCSDS synchronization markers, SDA markers and user-defined symbols. After a valid pattern has been detected, the bit-alignment and frame-extraction block determines the corresponding frame boundaries and separates the relevant data units for further processing. The signal-quality-assessment stage evaluates the integrity of the received stream using BER-related information, error counters, lock status and statistical indicators.

The recording and export block buffers the received data, transfers it to DDR or intermediate storage and provides either file-based or streamed output to the host system. Mission-specific decoding and detailed analysis are intentionally assigned to the software-based post-processing stage, thereby separating the high-speed acquisition functions from protocol-dependent modem processing.

The lower configuration and control path defines the data rate, synchronization pattern and operating mode used by the acquisition chain. In parallel, the monitoring and metadata path records timestamps, capture settings and system-health information and associates these data with the recorded stream. This structure provides the required configurability and observability while keeping the real-time FPGA implementation focused on deterministic reception, synchronization, quality monitoring and lossless data capture.

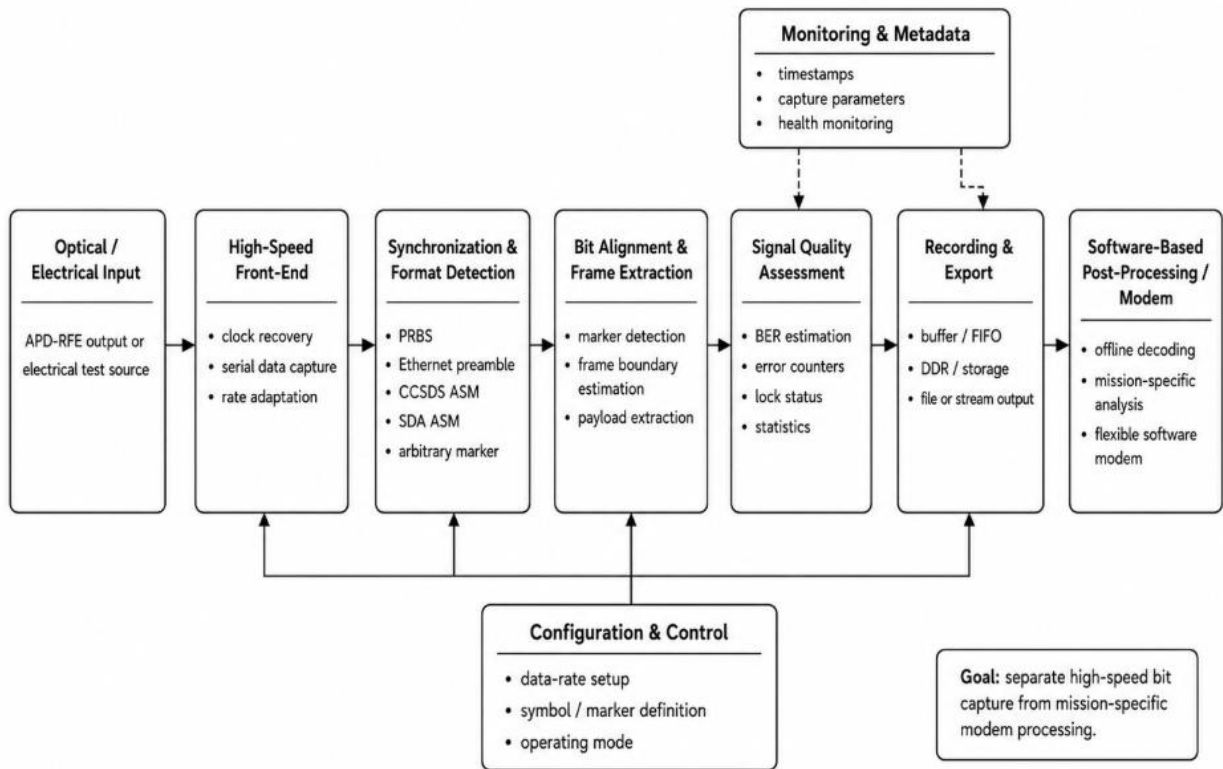


Fig. 7: End-to-end BSR processing chain

Signal quality assessment is an important step in evaluating the performance and reliability of optical communication systems. As the signal propagates through the channel, it is subjected to atmospheric turbulence, background noise, beam wander, tracking- and pointing-errors, and other optical interference. These effects introduce errors in the received signal, resulting in corrupted data or synchronization failure. Several performance metrics are employed by the BSR to evaluate the quality of the received signal:

- **Bit Error Rate (BER):** It is defined as the ratio of the erroneous bits to the total number of received bits. BER indicates the reliability of the communication channel. A lower BER indicates a more reliable communication link and improved system performance.
- **Frame Error Rate (FER):** The fraction of frames containing at least one erroneous bit. It indicates how frequently frames are affected by transmission errors.
- **Frame Loss Rate (FLR):** The ratio of frames that cannot be successfully recovered (e.g. by FEC) to the number of total expected frames. It can be caused by sustained synchronization failure or resource limitations (buffer overflow or interrupted data transfer). The metric is particularly important for continuous data recording. FLR is based on frames that cannot be recovered, whereas FER is based on frames that are recovered but may contain errors.

The online status and counter information generated by the BSR can subsequently be combined with offline BER and FER calculation, burst-error analysis, marker-miss and false-alarm evaluation, and bit-by-bit comparison on the host computer. Since atmospheric turbulence and pointing errors directly affect the end-to-end performance of CCSDS O3K links [6][10][15], these signal-quality functions are essential for interpreting link-test results.

5. BSR-IMPLEMENTATION AT AEROLiFi

The current prototype is based on an AMD ZCU106 evaluation board equipped with a Zynq UltraScale+ MPSoC and GTH high-speed serial transceivers. The implementation follows the architecture of Fig. 6, with time-critical reception and detection functions assigned to the programmable logic and control, buffering and host communication handled by the processing system. The prototype represents the first implementation stage of the BSR architecture targeting serial OOK reception up to 10 Gbit/s.

The validated high-speed receiver baseline was retained and incrementally extended with BSR-specific functions for synchronization, pattern monitoring, error assessment, metadata generation, and buffering. The intermediate-storage subsystem is intended to provide sufficient capacity for complete OLEODL acquisition sessions, including the recorded bit stream, associated metadata and buffering overhead. The final storage dimensioning will therefore be selected according to the required data rate and expected contact duration. A photograph of the FPGA platform and the connected intermediate-storage hardware is shown in Fig. 8.

In the first test configuration, predefined CCSDS synchronization patterns and PRBS sequences are generated by a bit-pattern generator. The generated serial pattern is applied to the FPGA and monitored with the oscilloscope. This configuration is used to verify the generated waveform, the electrical connection, the FPGA receiver lock and the correct reception of the test sequence. The PRBS sequence provides a deterministic reference for link validation and error counting, whereas the CCSDS pattern is used to verify synchronization-marker detection according to the symbol definitions summarized in Table 1.

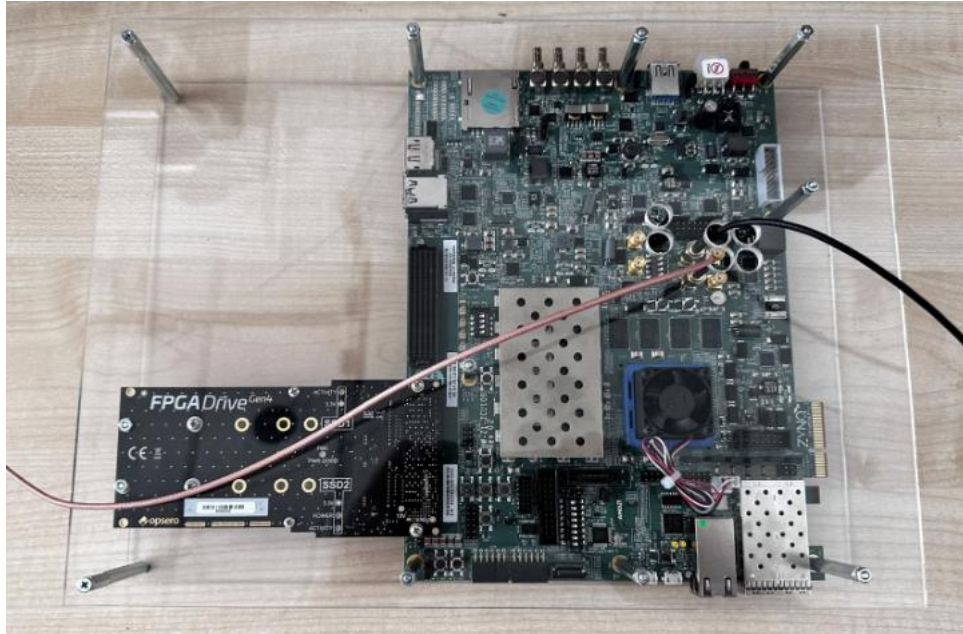


Fig. 8: Photograph of the BSR electronics with intermediate-storage hardware.

In the second test configuration, the 2.5 Gbit/s RFE is included in the signal path. The predefined test pattern is applied to the optical test path, received by the RFE and converted into a high-speed electrical signal. The electrical output of the RFE is applied to the FPGA and monitored with the oscilloscope. This configuration allows the complete path from optical reception through electrical conversion to FPGA acquisition to be evaluated.

The implemented testbed is shown in Fig. 9. It consists of a bit-pattern generator, the BSR FPGA platform, a 2.5 Gbit/s optical receiver front end (RFE), an oscilloscope and a control laptop. The control laptop is used to configure the bit-pattern generator and the measurement instruments and to monitor the FPGA. The oscilloscope provides an independent observation point for the electrical signals at different stages of the test chain.

The tests performed so far demonstrate the availability of the main laboratory infrastructure and the operation of the individual electrical signal paths. PRBS and CCSDS-type patterns can be produced by the bit-pattern generator, observed with the oscilloscope and applied to the FPGA input. The RFE output can likewise be routed to the FPGA and inspected independently on the oscilloscope. These measurements establish the basis for verifying receiver initialization, serial-data recovery and the integrity of the physical test path.

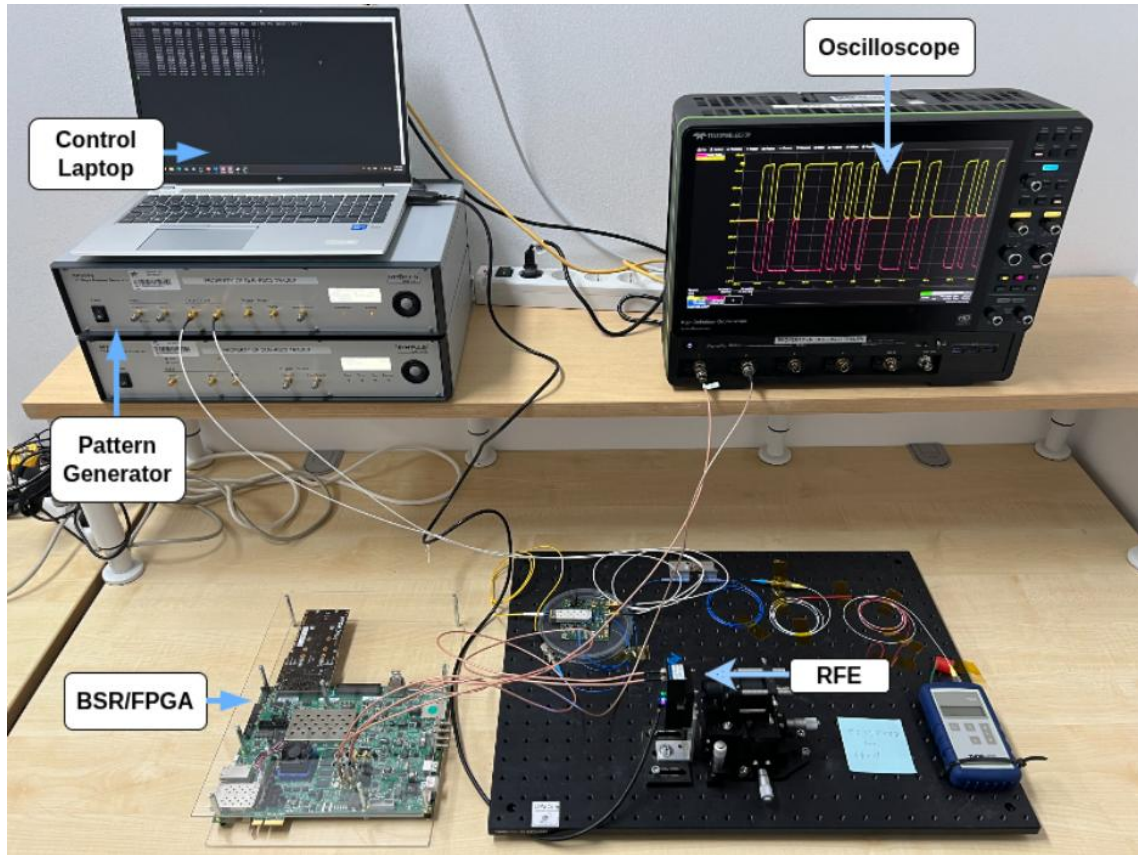


Fig. 9: BSR testbed setup

Subsequent measurements will evaluate receiver lock and recovery, BER-related statistics, marker misses and false detections, buffer integrity and sustained data transfer. After validation of the direct electrical path, the same procedure will be applied to the complete optical path using the 2.5 Gbit/s RFE, before even higher data rates will be covered.

6. CONCLUSIONS AND OUTLOOK

The interconnection of widely dispersed ground stations within a global network is a key strategy for mitigating cloud blockages in laser-based space-to-ground communications. Compatibility of the operators' own ground stations with current standards is therefore crucial when international collaborations are to be established. The bitstream recorder presented here offers a simple and cost-effective way of achieving this compatibility, although it is limited to only near-real-time transmissions. Its capability for initial signal analysis by real-time bit-error detection enables a rapid assessment of the channel characteristics of particular transmissions through the atmosphere. Moreover, performance analysis of the various space-based terminals is possible in a standardized way.

Satellite missions often implement different methods for dealing with atmospheric disturbances, i.e. different modulation formats and error correction mechanisms, use different portions of the available spectrum and transmit at different power levels. Furthermore, different projects pursue different strategies for signal acquisition and different orbital concepts (LEO, MEO, GEO). From a scientific perspective, it is of major importance to objectively compare the performance of these real-world implementations and concepts against one another - which is easily achieved using our bitstream recorder. Distinguishing itself from conventional data loggers by its ability to react on the various predefined packet formats, as well as

capture raw and unaltered digital data at extremely high speeds, it will be indispensable for applications where bit-level accuracy and timing are critical. Unlike general-purpose data loggers, it is designed to handle multi-Gbps throughputs with minimal latency, preserving the exact structure and timing of the input signal. Additionally, it incorporates deep, high-capacity storage in combination with advanced time-stamping capabilities of the signal quality, to ensure precise synchronization as is essential for debugging, protocol analysis, or post-processing tasks. In one of several application scenarios, it will enable DLR's “*Laser Bodenstation Trauen*” LaBoT [17] to work with various partner's space assets (figures 10 and 11).

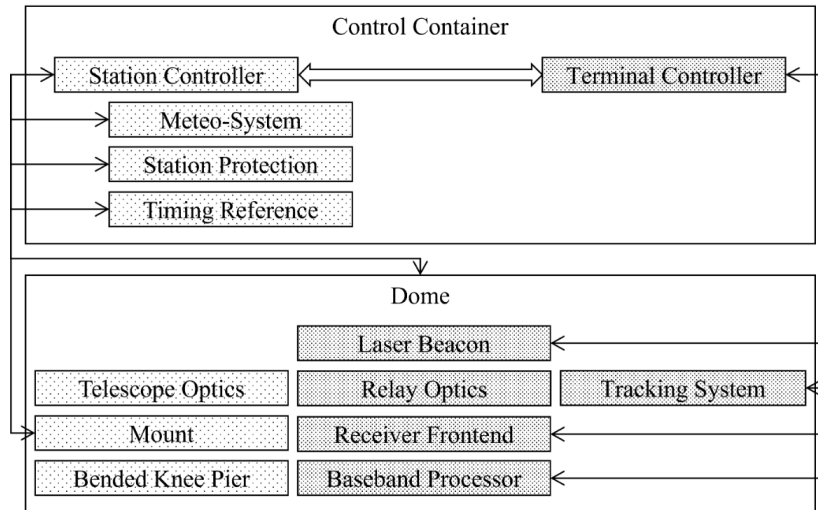


Fig 10: Functional block diagram of the LaBoT with its main building blocks.

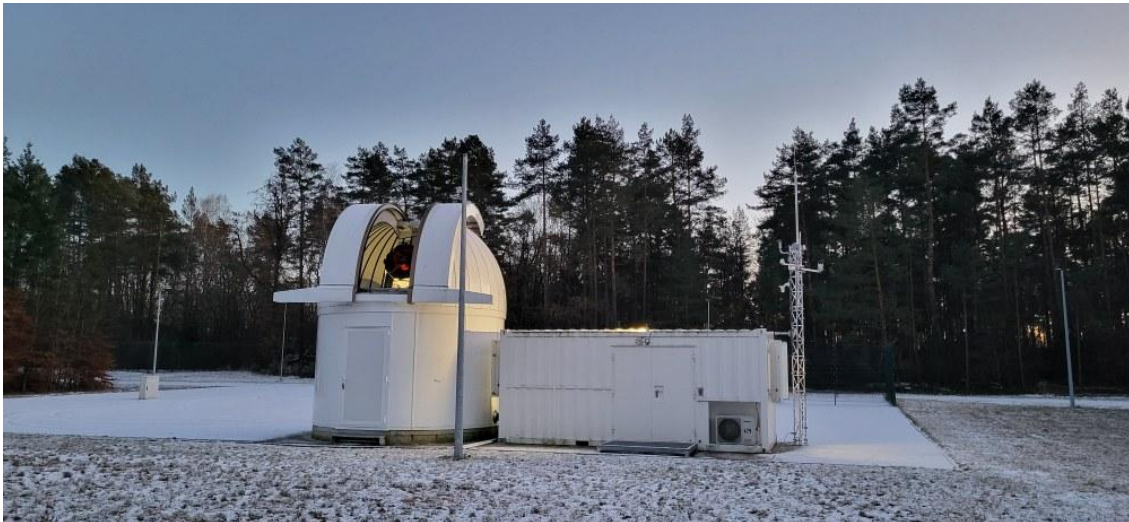


Fig 11: Target scenario of BSR usage is the DLR-OGS-Trauen [Credit: DLR (CC BY-NC-ND 3.0)]

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