

A scalable silicon photonic M-ary PPM transmitter using a cascaded MZI binary-weighted delay architecture

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ABSTRACT

Pulse-position modulation (PPM) is attractive for photon-starved space optical links because it concentrates the energy of each symbol into one short pulse. In a conventional transmitter the selected slot is produced by temporal pulse carving, requiring the modulator and its driver to resolve the slot period. We present a silicon photonic optical circuit switch that converts symbol into optical delay. A cascade of $\log_2 M$ Mach-Zehnder-interferometer (MZI) 2×2 switches selects delays of $T_{\text{slot}}, 2T_{\text{slot}}, \dots, (M/2)T_{\text{slot}}$, placing an input pulse in any of M output slots. The smallest delay is encountered first and the largest last; this ordering gives the final switch approximately half a frame in which to reconfigure after the preceding pulse has cleared it. Six variants spanning 4-ary to 64-ary PPM and 25–100 ps slots have been designed on a 220nm SOI platform. Depletion based switch addresses the short switching windows of the low-order variants, including an 8-ary, 25 ps design corresponding to 15 Gb/s, whereas lower-loss injection based switch are used for high-order variants up to 64-ary and 3.75 Gb/s. The architecture aims to separate the optical slot grid from the electrical update rate and offer a scalable route to multi-gigabit high-order PPM.

Keywords: pulse-position modulation, silicon photonics, space optical communication, Mach-Zehnder switch, optical delay line

1. INTRODUCTION

In M -ary optical pulse-position modulation, a symbol interval contains M data slots, and one pulse is transmitted in one of them, conveying $\log_2 M$ bits. Concentrating the symbol energy into one slot produces a high peak-to-average-power ratio and supports high photon efficiency with direct detection and photon-counting receivers.^{1,2} Figure 1 shows exactly that and compares PPM with on/off keying (OOK).

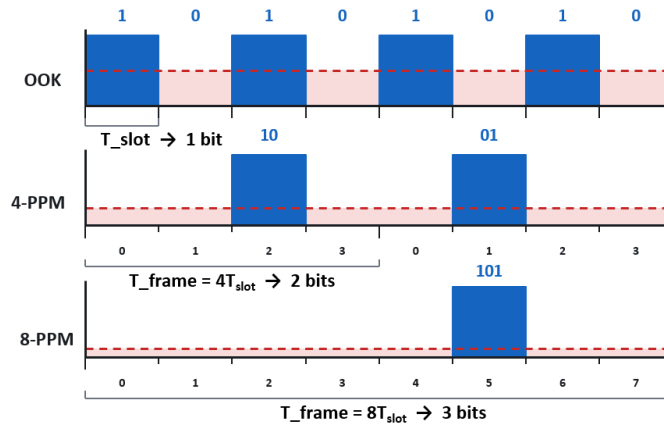


Figure 1. Comparison of PPM against on-off keying (OOK). The red line represents average power. As M scales the average power decreases.

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The associated reduction in spectral efficiency is comparatively acceptable for space links: vacuum propagation avoids the chromatic dispersion and nonlinearities of long fibre links, and the optical channel offers many terahertz of available bandwidth. PPM has consequently been used in NASA's Lunar Laser Communication Demonstration (LLCD) and Deep Space Optical Communications (DSOC) experiment.^{3,4}

Assuming no additional guard interval, and T_{slot} as the slot width the data rate (R_b) of a M-ary PPM is given by:

$$R_b = \frac{\log_2 M}{MT_{\text{slot}}}. \quad (1)$$

Most present transmitters create the occupied slot by gating a continuous-wave where the carving electronics must resolve T_{slot} , giving an architecture-level requirement $B_{\text{carve}} \geq 1/T_{\text{slot}}$, where B_{carve} is the required modulator bandwidth. At fixed R_b , this requirement grows as $M/\log_2 M$; equivalently, at fixed electrical bandwidth the achievable bit rate falls as $\log_2 M/M$. This is the central difficulty in combining high-order PPM with multi-gigabit data rates.

In order to solve this problem, there have been a couple of proposals. Birnbaum and Farr considered techniques very similar to the one that is proposed here to move the relevant timing precision from an individual modulator transition to the duration of the PPM symbol.⁵ Mendez *et al.* described a related 64-PPM cascade, but placed the largest optical delay first and also delayed the downstream electrical drive signals.⁶

Our method aims to solve the bandwidth bottleneck by designing an optical switching circuit where the bandwidth of the modulator is determined by the frame period rather than the slot period where frame period is defined as $T_{\text{frame}} = MT_{\text{slot}}$. The design consists of 4, 8, 16, 32, and 64-ary PPM which aims to show the scalability of the design. Section 2 explains the working principle, Section 3 the circuit level simulation, Section 4 implementing the design on 220nm SOI (Silicon on Insulator) platform, and Section 5 compares with other optical PPM transmitter design.

2. ARCHITECTURE AND TIMING

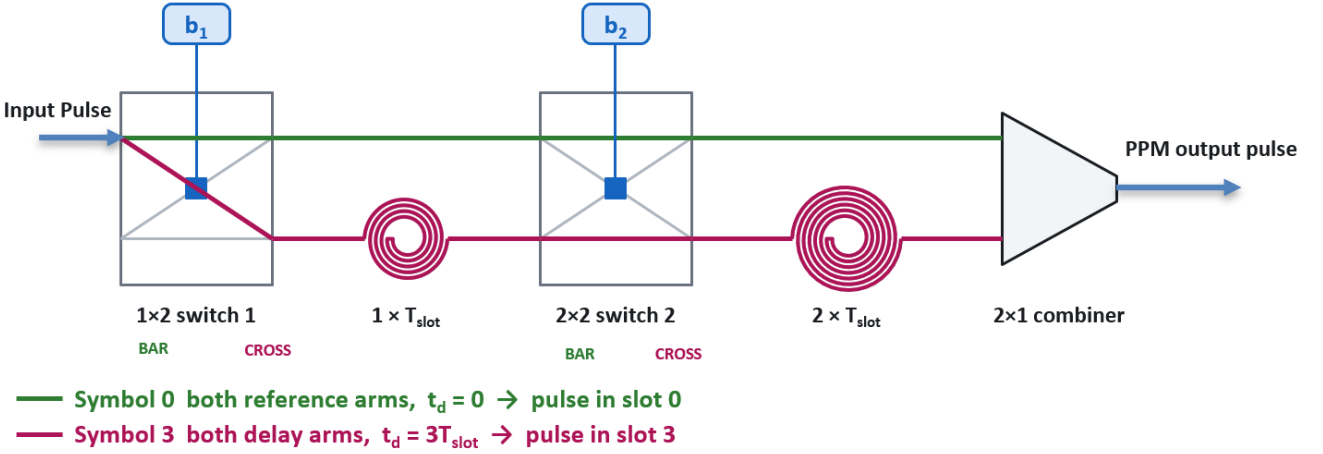


Figure 2. Schematic of a 4-ary PPM where b_1 and b_2 are driving the switch to switch between bar and cross port. Two example symbols are color coded to illustrate their path

Figure 2 is an example 4-ary schematic where the input pulse gets routed to one of the four routes based on the b_1 and b_2 drives. For $M = 2^K$, the transmitter contains one 1×2 switch and $(K - 1) 2 \times 2$ MZI switches. Stage i selects either a reference path with no delay or an excess delay (Δt_i) of length (ΔL_i).

$$\Delta t_i = 2^{i-1} T_{\text{slot}}, \quad \Delta L_i = \frac{c \Delta t_i}{n_g}, \quad (2)$$

where n_g is the delay-waveguide group index. The optical delay weights increase along the direction of propagation from T_{slot} to $(M/2)T_{\text{slot}}$. A 3 dB combiner joins the paths after the final delay.

If we assume a PPM scheme without any guard slot, the limiting case of this architecture is the transition from the last slot of one frame followed by the first slot of the next. Suppose that we start timing from the start of the first frame, the first pulse accumulates at most $(M/2 - 1)T_{\text{slot}}$ before reaching the final switch, whereas the next pulse of the following frame has to reach it just after MT_{slot} . That gives us a switching window of ($T_{\text{switching}}$):

$$T_{\text{switching}} = \left(\frac{M}{2}\right) T_{\text{slot}}. \quad (3)$$

Assuming a modulator capable of transitioning its state (on/off) we will have a bandwidth of at least $1/(MT_{\text{slot}})$. For example in a 64-PPM, $T_{\text{slot}} = 25$ ps, $T_{\text{frame}} = 1.6$ ns and $R_b = 3.75$ Gb/s., the pulse carving modulator would need to have a bandwidth of about 40 GHz compared to less than 1 GHz in this case.

Another important aspect of this architecture is that each pulse traverses a MZI only after the switch state has settled into BAR or CROSS state. Therefore the relevant metric is the settled-state extinction ratio at the actual drive voltages, rather than the dynamic extinction measured while the switch is transitioning. This avoids the pulse overlapping an incomplete phase transition. Thermo-optic phase shifters can be used to tune phase imbalances for an improved extinction ratio as shown by.⁷

3. CIRCUIT-LEVEL SIMULATION

As the architecture aims to show the scalability of the solution, there are six variants of PPM in this design (Table 1). For example within 16, 32 and 64-ary PPM, as M increases data rate increases because T_{slot} is decreasing, but since the frame rate remains constant the modulator bandwidth requirement remains the same. These design were laid out on a single 11.47 x 4.9 mm die for the CORNERSTONE 220 active SOI platform⁸ and submitted for fabrication.

Table 1. Transmitter variants laid out and submitted for fabrication.

Variant	M	Stages	T_{slot}	T_{frame}	R_b	MZI family
1	4	2	50 ps	0.20 ns	10.00 Gb/s	depletion
2	8	3	50 ps	0.40 ns	7.50 Gb/s	depletion
3	8	3	25 ps	0.20 ns	15.00 Gb/s	depletion
4	16	4	100 ps	1.60 ns	2.50 Gb/s	injection
5	32	5	50 ps	1.60 ns	3.125 Gb/s	injection
6	64	6	25 ps	1.60 ns	3.75 Gb/s	injection

Lumerical interconnect software⁹ is used to do a circuit simulation. The simulation is an architecture-level, literature-parameterised study intended to evaluate temporal routing, accumulated loss and leakage. Each MZI is represented by a 2×2 transfer function with prescribed insertion loss, settled extinction ratio, electrical transition time and ideal 0 and π switching states. The results therefore demonstrate circuit operation conditional on the specified component performance.

Switch parameters assumed in the simulation are taken from literature. The injection assumptions are anchored to reported forward-biased PIN modulators. Dev *et al.* demonstrated a foundry-fabricated 50- μm MZM with $V_\pi L = 0.0025$ V-cm, 1.2 dB insertion loss, 30 dB heater-tuned static extinction, and 5 Gb/s NRZ operation without pre-emphasis.⁷ They also estimated an approximately 1 GHz RC cut-off from the simulated junction resistance and capacitance, while nevertheless demonstrating 5 Gb/s NRZ operation without pre-emphasis.⁷ Akiyama and Usuki obtained a similar cut-off in a lumped forward-bias model, above which the response decreases approximately as $1/f$; using pre-emphasis, they demonstrated 56 Gb/s operation in a ring-resonator modulator.¹⁰ Because every pulse traverses settled switches, static extinction is used and is conservatively bounded by the -17 to -34.5 dB settled crosstalk of demonstrated injection 2×2 switches.^{11,12} Similarly for depletion mode, comparable 1-mm push-pull depletion phase shifters report $V_\pi L = 1.4$ – 2.7 V-cm, approximately 4 dB/mm loss, and operation at 40–52 Gb/s.^{13,14}

Passive assumptions are $n_g = 3.803$ and 0.5 dB/cm for the delay waveguide, 0.01 dB per taper, 0.02 dB per bend, and a 3 dB fundamental penalty at the passive output combiner.

Figure 3 is the simulation result of 16-ary design. All of the pulses arrive correctly. The farther slots experiences more delay so they accumulate more loss primarily due to propagation loss and also bends and tapers. The power out of unwanted slots are termed as ghost pulses here. This arises mainly from finite extinction and also an adjacent-slot can contain the selected pulse tail. The insertion loss in this case including 3 dB combiner loss and excluding the coupling is 8.2 dB for slot 0 and 14.63 dB for slot 15. For each symbol, the selected-to-largest-ghost ratio is given by $10 \log_{10}(P_{\text{selected}}/P_{\text{largest ghost}})$; its minimum over the 16 symbols is 10.12 dB (as shown in figure 3(b)).

To illustrate the switching states, consider slots 00 and 15 in Figure 3. For slot 00, the pulse follows the reference path at every stage, so all four switches are in the BAR state. For slot 15, the first switch changes the pulse from the reference-side input to the delayed path and is therefore in the CROSS state. The pulse then enters each subsequent switch through the delayed-side input, where the BAR state keeps it on the delayed path. Slot 15 therefore requires the sequence CROSS-BAR-BAR-BAR, as shown at approximately 16 ns in the figure.

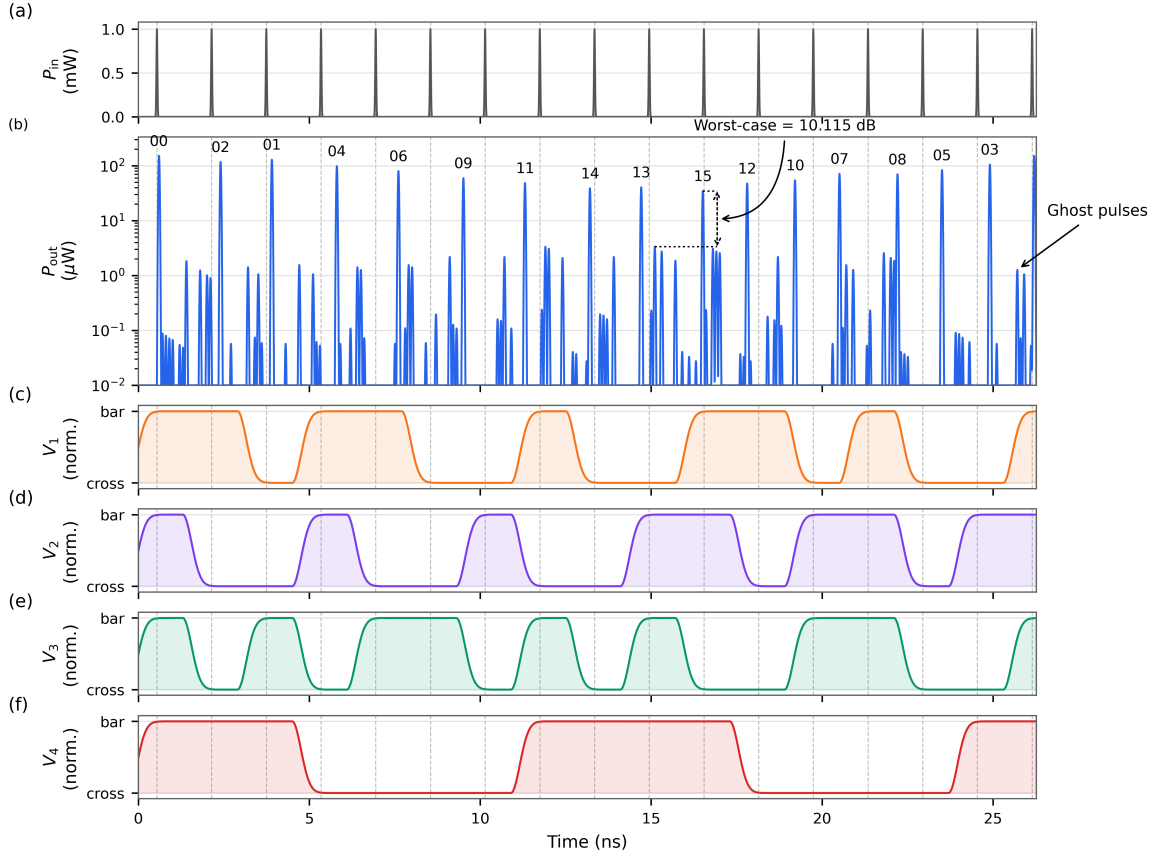


Figure 3. 16-ary PPM. (a) Input pulse operating at frame rate (625 MHz). (b) Output pulse at different slots of the frame. (c), (d), (e) and (f) are the two states namely bar and cross of their respective stage.

4. PHOTONIC INTEGRATED CIRCUIT IMPLEMENTATION

Depletion mode modulator is used for low ary PPM for higher data rate purpose. The insertion loss of the modulator limits its scalability for higher ary PPM. Thus injection mode modulators are used for 16, 32 and 64-ary PPM. They trade off speed with lower loss and lower operating voltage, substantially decreasing the complexity at the electronics driving side compared to depletion. Rib waveguides are used in the lateral PN/PIN phase shifters, compact single-mode strip sections are used through bends and routing, and the long delay straights use $2 \mu\text{m}$ -wide multimode strip waveguides. Widening reduces sidewall interaction and hence scattering loss; $2 \mu\text{m}$ silicon spirals with calculated sidewall-scattering loss of 0.042 dB/cm and estimated total scattering near

0.25 dB/cm have been reported.¹⁵ The present simulation model assumes a 0.5 dB/cm delay line propagation loss, and adiabatic rib-strip and single-mode-multimode tapers connect the different sections. Each MZI includes a heater for phase balance.

The largest individual delay is 800 ps in the 64-PPM circuit, corresponding to approximately 63.1 mm at $n_g = 3.803$; the all-delay path contains approximately 124 mm of excess waveguide. Switch count grows only as $\log_2 M$, but the total selected delay, propagation loss and path-to-path non-uniformity grow much faster. The layout therefore also contains balanced/unbalanced MZIs and dedicated delay, taper and bend test structures so that active and passive losses can be separated after fabrication. The two outputs after the final delay are joined by another MZI stage. Figure 4 shows the layout implementation for 4-ary depletion mode design. Figure 5 (a) shows the layout implementation for 16-ary injection mode design; (b) shows the zoomed single stage switch.

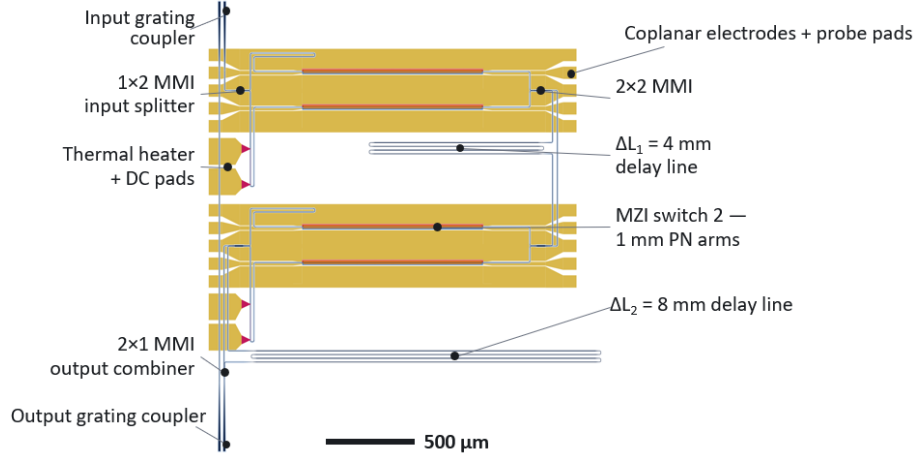


Figure 4. Layout of 4-ary depletion mode modulator with two depletion mode modulator with delay lines and input and output coupling.

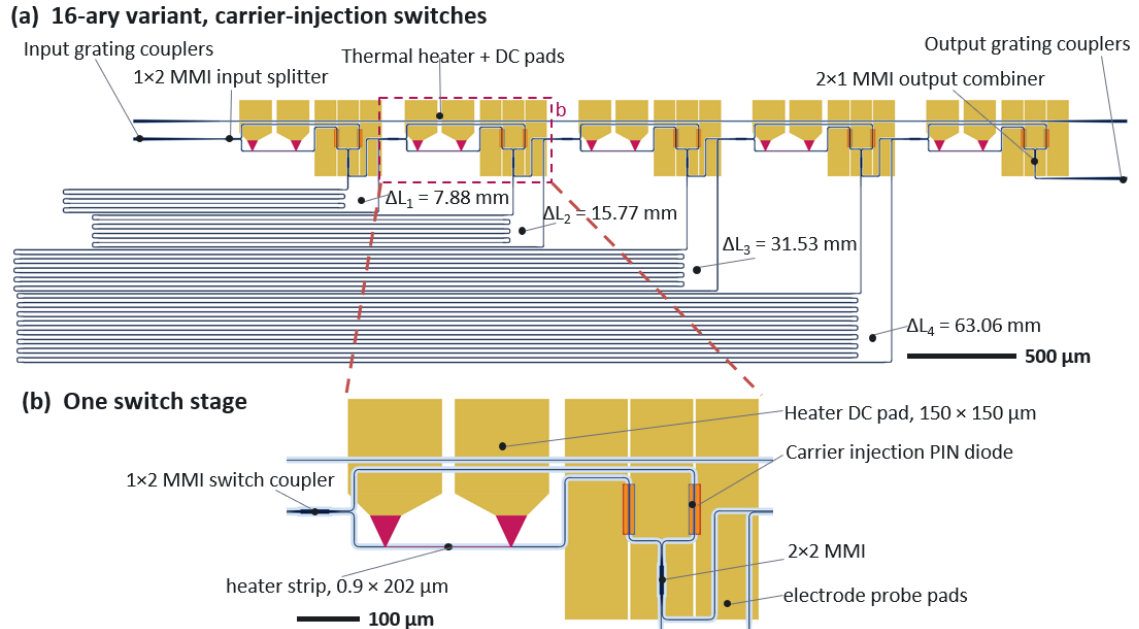


Figure 5. 16-ary layout. (a) Layout of 16-ary injection mode modulator with 4 stages of injection modulator for circuit switching and additional stage as a combiner. (b) A single stage switch.

5. COMPARISON WITH OTHER DESIGN

Table 2 compares the performances of flight demonstrations, integrated-photonic implementation and from the present untested design. The InP demonstrations from the Rosborough *et al.*¹⁶ are the closest experimental PIC comparators: the 2016 circuit generated wavelength-tunable 16-PPM with 28 dB extinction, while the later high-power PIC integrated a DBR laser, SOAs and an EAM and demonstrated 16-PPM at 1.25 Gb/s with 9.6 dB extinction.¹⁷ In both cases slot position is produced by temporal intensity modulation; here it is defined by passive delay and spatial routing.

Table 2. Comparison with existing PPM transmitter implementations.

Transmitter	Platform and slot-generation method	Reported FOM(Figure of Merits)
LLCD ³	Flight MOPA transmitter; temporal pulse generation on a 5 GHz slot grid	16-PPM; variable slot rate from 39–622 Mb/s (4.976 Gslot/s at 622Mb/s)
DSOC ⁴	4 W flight laser transmitter; temporal PPM generation	SCPPM; up to 267 Mb/s at 0.37 AU
Rosborough <i>et al.</i> ¹⁶	Monolithic wavelength-tunable InP transmitter; integrated intensity modulation	16-PPM; 28 dB extinction; 8 nm tuning
Zhao <i>et al.</i> ¹⁷	InP DBR laser, SOA, EAM and booster SOA; pulse carving	16-PPM; 1.25 Gb/s; 9.6 dB extinction
This work	SOI MZI switch cascade, ascending binary delays and 3 dB combiner	4–64 PPM; 2.5–15 Gb/s design points

6. CONCLUSION

A cascaded MZI circuit with ascending binary-weighted optical delays has been proposed that can map a $\log_2 M$ -bit to one of M pulse positions without requiring the switch drive to generate the slot duration. Six 4- to 64-PPM variants have been laid out and submitted for fabrication. Depletion switches provide the short transition time required by the low-order/high-rate circuits, while lower-loss injection switches make the longer high-order cascades more practical. The 64-PPM design at 25 ps slot time is capable of up to 3.75 Gb/s information rate.

This paper presents a device design and circuit simulation model based on expected performance parameters like accumulated switch, delay loss and coherent leakage, but does not include short-pulse dispersion, fabrication error, thermal drift, packaging and electrical drive. Scaling ultimately depends on a switch that combines low insertion loss, high settled extinction and sufficiently fast reconfiguration, together with lower-loss delay waveguides. Such components could extend the architecture to substantially higher PPM orders and make photon-efficient PPM useful not only for deep-space links but also for cislunar and shorter-range multi-gigabit optical communication.

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