# GMVISION CO-PROCESSOR FOR COMPLEX VISION-BASED AUTONOMOUS NAVIGATION IN SPACE

**D. G. Gogu, C. Mihalache, A. Stancu,[(1)], M. Casasco, O. Dubois-Matra, D. M. Codinachs, F. Vollaro [(2)], J.Wajoras[(3)]**

*[(1)] GMV Innovating Solutions S.R.L, Bucharest, Romania*
*{dgogu.ext, calin.mihalache, fstancu }@gmv.com*
*[(2)] European Space Agency – ESTEC, The Netherlands*
*{massimo.casasco@esa.int, olivier.dubois-matra@ext.esa.int, david.merodio.codinachs@esa.int, fabio.vollaro@ext.esa.int}*
*[(3)] GMV Innovating Solutions Sp. z o.o., jwajoras@gmv.com*

## ABSTRACT

As space exploration missions continue to push boundaries, the demand for advanced navigation algorithms and their implementation in avionics modules and data interfaces is escalating. To meet the autonomy and reliability requirements of modern space missions, vision-based navigation utilizing high-resolution images processed onboard at high frame rates has become essential. The complexity of computer vision algorithms and the fusion of data from diverse onboard instruments and sensors necessitate the development and utilization of high-performance avionics capable of executing computations one or two orders of magnitude faster than conventional space-grade processors.
Consequently, significant efforts are currently being devoted to the development of high-frequency, high-accuracy navigation systems, minimizing spacecraft power consumption, and optimizing processing times for near real-time operations. This paper focuses on the development of GMVision, a highly versatile space-oriented image processing unit designed to facilitate the interfacing, control, and management of up to eight SpaceWire links. Furthermore, GMVision offers the integration of computationally intensive image processing algorithms, providing various redundant vision-based navigation solutions for autonomous operations in space missions.
Those image processing algorithms solutions have proven effective for applications such as rendezvous-search-capture, active debris removal, in-orbit servicing, descent and landing on small or massive celestial bodies, and rover exploration.
This paper introduces GMVision, a highly versatile space-oriented image processing unit designed to address the evolving requirements of space missions. Notably, GMVision provides a unique capability for reprogramming algorithms and adapting navigation strategies in real-time, even while the spacecraft is in flight. By integrating state-of-the-art image processing algorithms and leveraging the vast computational power of GMVision.

Keywords: On-board processing, FPGA, On-board reprograming, Image navigation, space, microelectronics, equipment.

## 1 INTRODUCTION

As current and future space exploration missions are getting bolder, so do the requirements on the navigation algorithms and subsequently on their implementation in the avionics modules and on the associated data interfaces. To achieve the high level of autonomy and reliability required in today's space missions, vision-based navigation making use of high resolution images and processed on-board at high frame-rates is mandatory. The increased complexity of these computer vision algorithms and the data fusion of measurements acquired from various on-board instruments and sensors mandate the development and use of high-performance avionics to provide one or two order of magnitude faster execution than today's conventional space-grade processors. As consequence, nowadays substantial efforts are done to develop high frequency, high accuracy navigations systems, to improve on-board spacecraft power consumption and to optimize the processing times of the computational loads to achieve near real time operation.
The GMVision board can provide various redundant Vision-based Navigation solutions for autonomous operations in space missions, as GMV has previously developed within different ESA activities (CAMPHORVNAV, NEOGNC-2, Lunar-Lander, PILOTB+, HERA, HIPNOS, ORCO, NEOSHIELD, HERACLES or Mars Sample Return) several

image processing algorithms and navigation filters based on autonomous relative or absolute navigation, suitable for rendezvous-search-capture, active debris removal and in-orbit servicing, descent and landing into small or massive bodies or to accommodate computer-vision solutions for rover exploration.
The image processing board can adapt to different redundancy concepts, depending on mission needs or system requirements. The GMVision system provides 2 boards isolation for Image Processing Function and Interfaces function, as it is relying on a two FPGAs architecture for each board. Both FPGAs are rad-hard European BRAVE units with allocated external volatile and non-volatile memories: an NG-MEDIUM dedicated to interfaces control unit and monitoring, and a powerful NG-LARGE to perform as computer vision co-processor. The image processing algorithms functionality can be divided between the processing FPGA and a SW processor, making use of a HW/SW co-design approach, as GMVision can be interfaced via SpaceWire with an On-board computer. This is the case for the two use-case scenarios for the development of GMVision Mars Sample Return mission concept Vision-Based GNC Rendezvous with ERO platform or Lunar lander with both absolute and relative navigation.
The SpaceWire interfaces allow TM/TC exchange between GMVision and up to 3 devices/instruments using nominal and redundant SpaceWire links (nominal/redundant 1 on-board computer and 2 navigation cameras or eventually 8 different instruments). GMVision system can also include pre-processing functions for the navigation cameras or other sensors, as well as managing the redundancy concept.
The high performance, fast and complex computer vision solutions are focused on the needed processing, so both FPGAs of the board are SRAM reprogrammable devices which allow flexibility and many options for the design and implementation of complex functionalities, such as high-data rate interfaces management and hardware accelerators. Thanks to the reprogramming capabilities it can also be possible to accommodate different computer-vision accelerators which are not used in the same moment of time by replacing partially or fully bitstreams in the processing FPGA to save a potentially needed second FPGA unit.
The GMVsion concept is promising technology, and it has high exploitation applicability also to other missions, such as Lunar Missions with Roadmap as a Smart sensor. Being reference architecture for complex high-performance algorithms, the product is a feasible solution for space-based surveillance system, or to the Mars exploration missions.
The HW/SW co-design architecture is developed around a Design, Development, Verification and Validation (DDVV) plan with the objective to ensure complete testing of system. The validation chain is based on the following test benches: model in the loop (MIL), processor in the loop (PIL), FPGA in the loop (FIL) and hardware in the loop.

# 2 SCENARIOS

Two navigation scenarios with two use cases each were chosen for the activity to validate the solution. An in-orbit rendezvous scenario based on Mars Sample Return mission, which covers both far and close approach to the Orbiting Sample (OS) and uses two cameras: Wide Angle Camera (WAC) and Narrow Angle Camera (NAC). A landing scenario based on PILOT lunar landing with absolute and relative vision-based navigation algorithms running side-by-side using WAC.

## 2.1 In-orbit rendezvous

The use cases in the rendezvous scenario cover Long Range Image Processing (LRIP) with WAC (approx.630-240m of range to the OS) and Short Range IP (SRIP) with NAC (approx.140-100m of range).

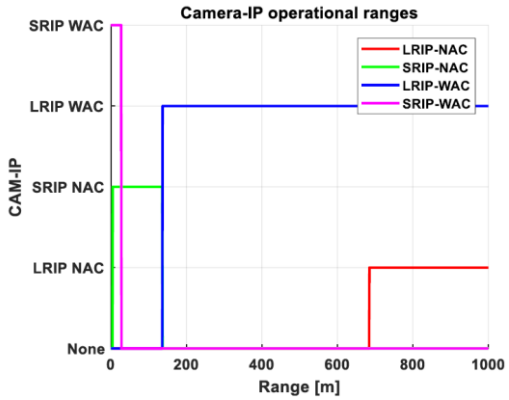



Figure 1. Rendezvous camera and IP combinations and corresponding operational ranges

Two IP algorithms are used: faint object detection for LRIP and silhouette matching for the SRIP.

A Long Range Image Processing (LRIP) based on disparity check analysis permits to distinguish the OS from the stars in the background during target pointing attitude profiles. LRIP algorithm stages:

- Stage 0: Image acquisition and radiometric correction.
- Stage 1: Image binarisation
- Stage 2: Candidate screening
- Stage 3: Screened frame analysis.
- Stage 4: Centroiding of the target object(s).

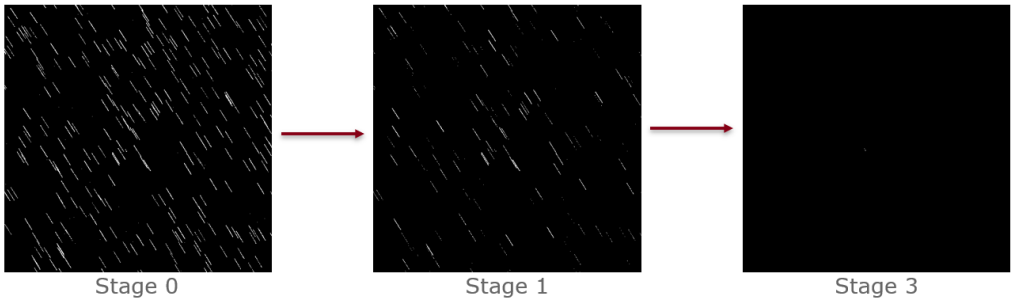



Figure 2. LRIP algorithm stages

The SRIP is based on silhouette descriptors technique, which permits to identify the shape of the OS (and so determining its distance and centre Line of Sight) under different illumination conditions.

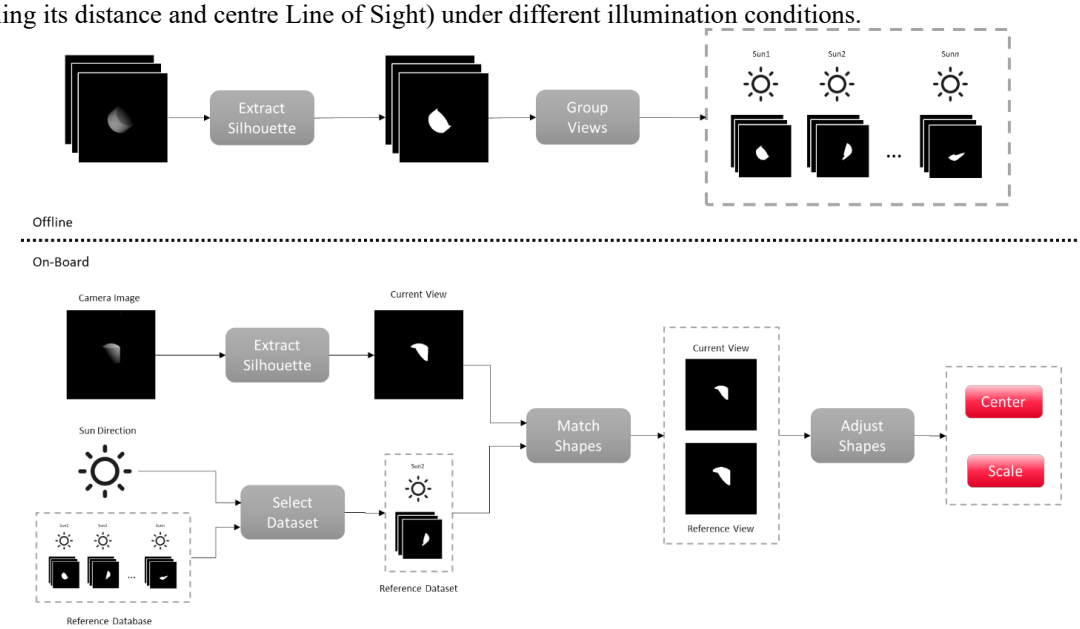



Figure 3. SRIP algorithm functional break-down

## 2.2 Lunar landing

In Lunar landing scenario both absolute and relative IP algorithms are used during Low Lunar Orbit phase with WAC (100km above ground) during trajectory over vicinity of the South Pole.

**AbsNav** extracts and compares visible Lunar landmarks with offline extracted landmarks database and yields absolute positions of matched landmarks in Planet Centered Planet Fixed frame and their positions in the image frame.

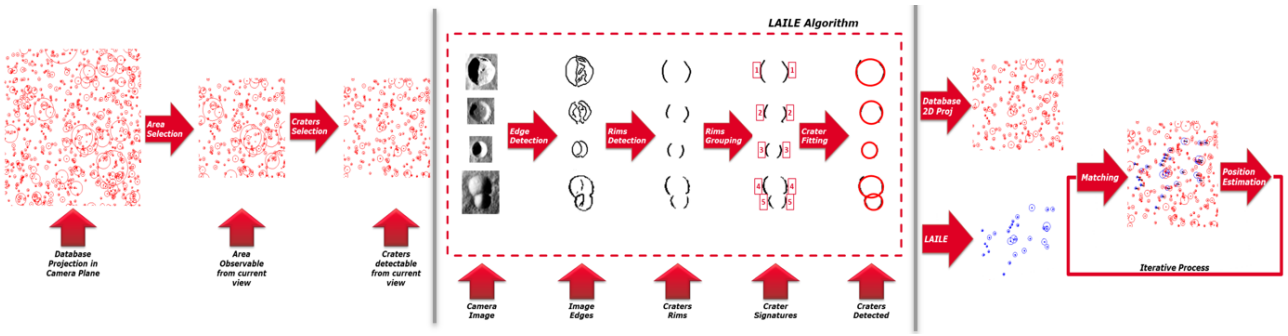



Figure 4. AbsNav algorithm functional break-down

The functioning principle of the RelNav algorithm is extracting features from an image. The features are then compared with the features extracted in previous image frame in order to find correspondences, performing feature tracking.

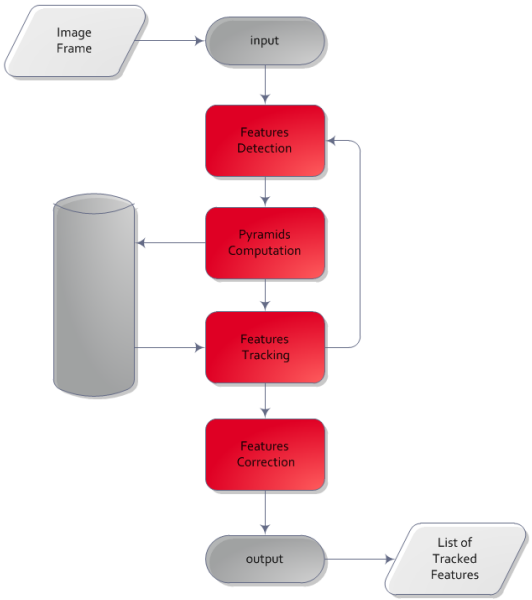



Figure 5. RelNav algorithm functional break-dowm

## 3 AVIONICS SYSTEM ARCHITECTURE

For the GMVision activity, the avionics was re-designed from CAMPHORVNAV based on the project requirements. The architecture evolved during the project where a baseline was composed by an image processing board (IPB) where the main active components are European based. The final architecture it is validated using two CMOS based cameras developed during MSR-DD [2] and CAMPHORVNAV [1] activities as show in the below architecture.

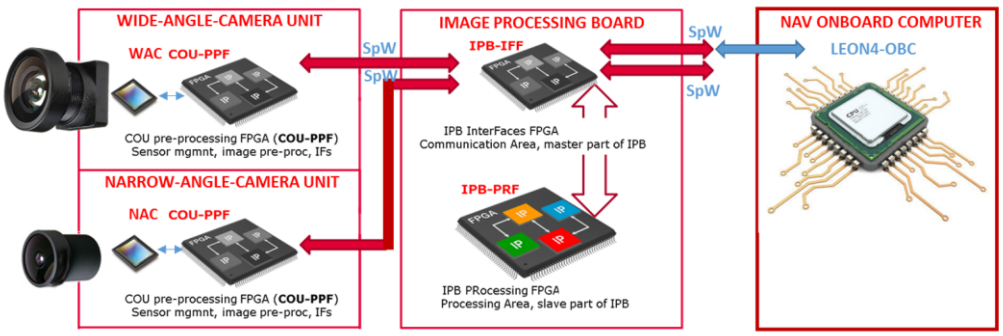



Figure 6. GMVision architecture

Dedicated development of new avionics technologies is driven by the needs of all areas of space applications for image processing using two camera optical head units linked by means of SpW interface with nominal and redundant connection. The dedicated avionics include two rad-hard FPGA, European NG-MEDIUM and high-performance NG-LARGE.
NG-MEDIUM oversees both the external/internal interfacing. The concept is an evolution of Image Processing Board as previously being developed in different GMV activities [1] but including in this case also the capability to control and command two camera logic. Avionics incorporates a second FPGA dedicated to the implementation and HW-acceleration of the computer- vision algorithms, the most computationally demanding part. The FPGA high performance solution allow more consecutive frames being processed thanks to the utilization of FPGA and the pipeline processing in streaming of the cameras images acquisition in the presented embedded HW solution.

The key HW modules can be summarized as follows:

- Power Input module,
- Interface Communication Control,
- Data Processing Control module.

The impact of a significant miniaturization of avionics system has been studied in the framework of a complete solution for providing redundancy in the same enclosure. In order to reduce the risks, the avionics was split in two identical PCBs in the same enclosure communicating between them using differential pairs inside NG-MEDIUM.
The effect of combining the traditional avionics elements in a complete system has been analyzed, and the impact on avionics mass, power, volume, operability, complexity, risk, and cost for the avionics architecture has been studied.

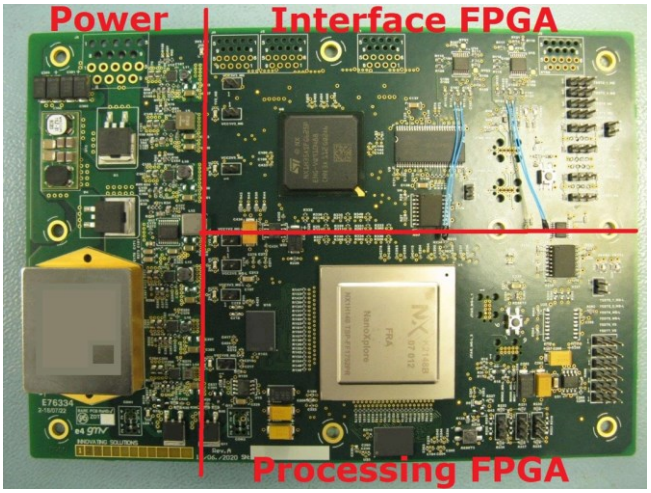



Figure 7. Re-designed IPB

The avionics module board architecture is composed of two different interconnected main areas:
- Data Interface Communication Control, which the NG-Medium FPGA as the main processor. This area is connected to the interface of the system and controlling both power outputs lines.
- Data Processing Control, withs the NG-LARGE FPGA as the co-processor. This area is used for high-performance image processing.

For storing the captured images and various maintenance services, the NG-Medium FPGA uses a SDR SDRAM memory.
For supporting the processing algorithms, DDR2 memory is selected. The part will allow fast transfer by using dual data rate and burst functionalities.
Data exchange between the Data Interface Communication Control and the Data processing module is enabled by parallel interface using a full duplex 8bit transmission solution. The solution requires at least 23 connections for the link between the two FPGAs.
The avionics is interfacing using nominal and redundant SpW links with the OBC, nominal and redundant SpW with two instruments such as cameras units. and it can provide power supply to each instrument with the power output lines with the capabilities of 5V @ 1 A per Link.

# 4 HW/SW IMPLEMENTATION

The visual based system development, integration and testing is relying on the so-called SW V lifecycle, [4], adapted to fulfil the objectives of HW/SW co-design and integrates all the DDVV test benches which ensures the interconnection between all design phases:

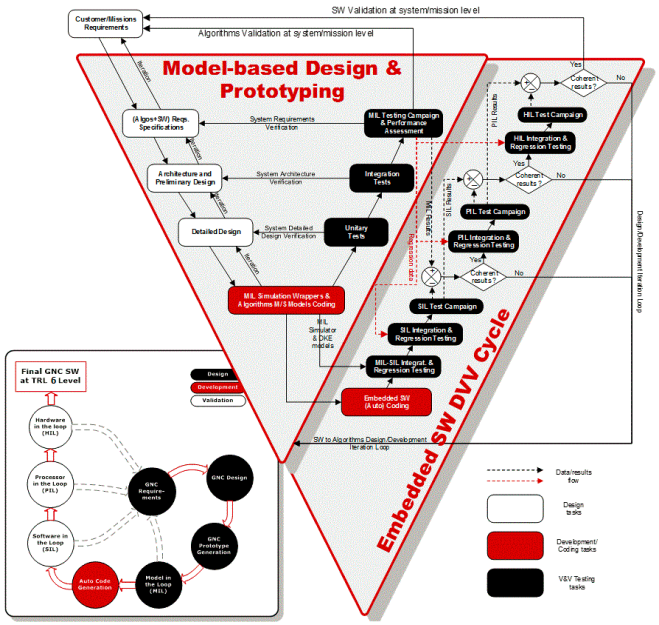



Figure 8. Visual-based system development cycle, [4]

On key step is represented by the co-design partitioning process, where the computer vision algorithm is split in SW and HW part (Figure 9). During this step the SW version of the computer vision algorithm is analyzed to decide which submodule are proposed to be ported on a dedicated acceleration HW. For this purpose, the SW submodules are analyzed from different perspective, such as: time execution, memory consumption and integration feasibility on the acceleration HW. Depending on the integration feasibility and HW resources, the co-design process could lead to a full HW solution of the computer vision algorithm or to a HW/SW co-design. Most often the feasible solution proved to be a HW/ SW co-design, which is also the case of GMVision. In the co-design approach part of the computer vision algorithm is executed in SW and HW in accordance with the architecture decided during the co-design process.

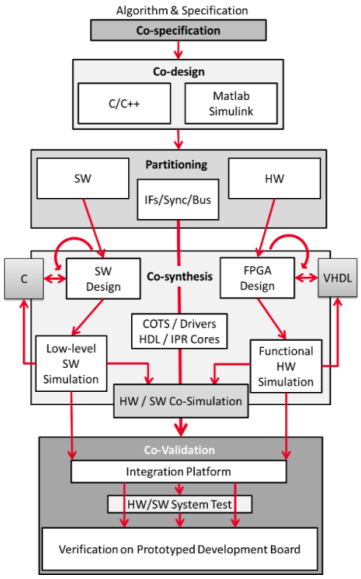



Figure 9. HW/SW co-design process, [5]

The SW part is running on a LEON4 processor using RTEMS operating system. The setup is fully representative,

LEON4 being a fault-tolerant quad-core processor. The LEON4 is integrated in dedicated electrical ground support equipment (EGSE), build specifically for image processing HW accelerator testing. The EGSE is built as an independent rack which contains a power supply, a dedicated workstation, a E698PM-DKIT v2.0 and an emergency button. The SW submodules proposed for HW acceleration are ported on VHDL and executed using the IPB. The interfaces between the SW and HW elements are established via SPW connection.


Figure 10. HW/SW codesign integration and testing setup

The configuration presented in Figure 5 is used to test all four computer vision algorithms. The host PC is in charge to ensure the necessary inputs to test the HW/SW co-design and to obtain the results for validation purposes.

# 5 MECHANICAL HW DESIGN & MOUNTING

The enclosure structure is designed to accommodate all the electronics. The redundancy of the system is delivered by a second IPB unit which communicate via dedicated differential pairs with the communication FPGA.

The design has been realized taking into account the general requirements defined by ESA, the space mechanical design consideration, the IPB PCB and selected components and the fabrication methods based on ECSS standard which are the most common standards to be followed for space units manufacturing.
Each of these requirements impact differently in the mechanical design and its parts, in fact, some parameters such as the material, the mounting hole size, the weight optimization method chosen, the size and the final shapes are defined by the requirements. The final shape of the enclosure has been manufactured with AL 6082-T651 with a surface treatment of black anodizing, where the total mass is approx. 2.7 Kg, where the envelop is 300 mm x 180 mm x 59 mm (Figure 12 ). All the connectors are available on one face of the enclosure and with 4 x M4 mounting holes. The mechanical enclosure is composed of a Baseplate ( used to fix the unit to the S/C and it is considered a critical part for the thermal dissipation), Top Cover (it is mounted on the top of the baseplate and it used to close and seal the enclosure), Stiffeners (used to fix the electronics and increase the rigidity of each PCB and to fix them to the enclosure, baseplate or top cover) and the dissipation foils (used to increase the thermal dissipation and to conduct through convection the heat generated by the FPGA to the enclosure walls).

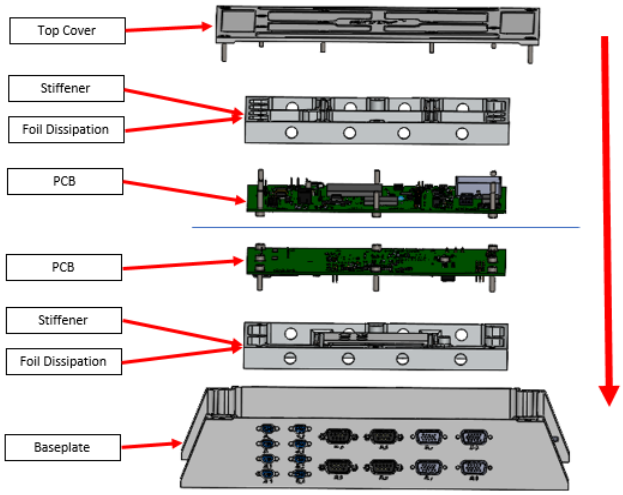



Figure 11. GMVision Unit, Explode view.

In the following figure it is presented the final HW assemby. Where the MDM9 connectors have been selected for SpW interface and for the power input, power output DB9 connector is available. Since the unit is an TRL 6, the JTAG infterfaces for both FPGAs was considered to be added into the front panel by means of DB15 high density, this interface can be removed for higher TRLs with no impact or minimum impact with respect to the enclosure structure from mechanical or thermical point of view.

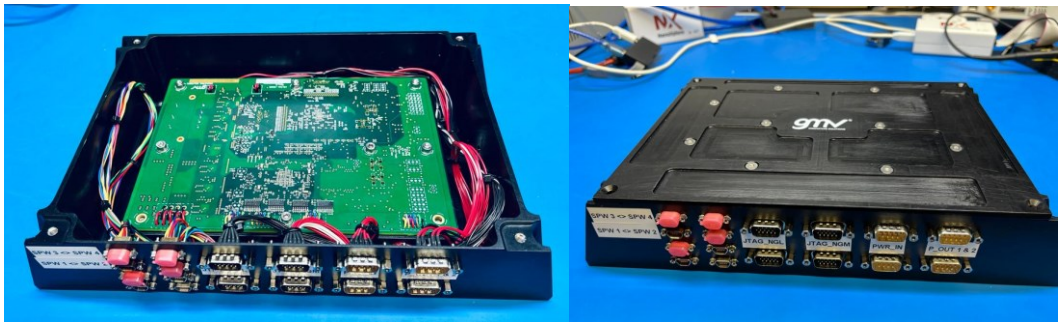


Figure 12. GMVision Unit

# 6 IPS HW TESTS

## 6.1 Model in the loop MIL

Baseline scenarios use synthetic images generated in PANGU environment. The rendezvous scenario use OS model and backed-up by star background in case of LRIP. Images are acquired and processed every 4 seconds in both cases.

| Long range rendezvous (contrast enhanced for presentation) | Short range rendezvous |
|---|---|

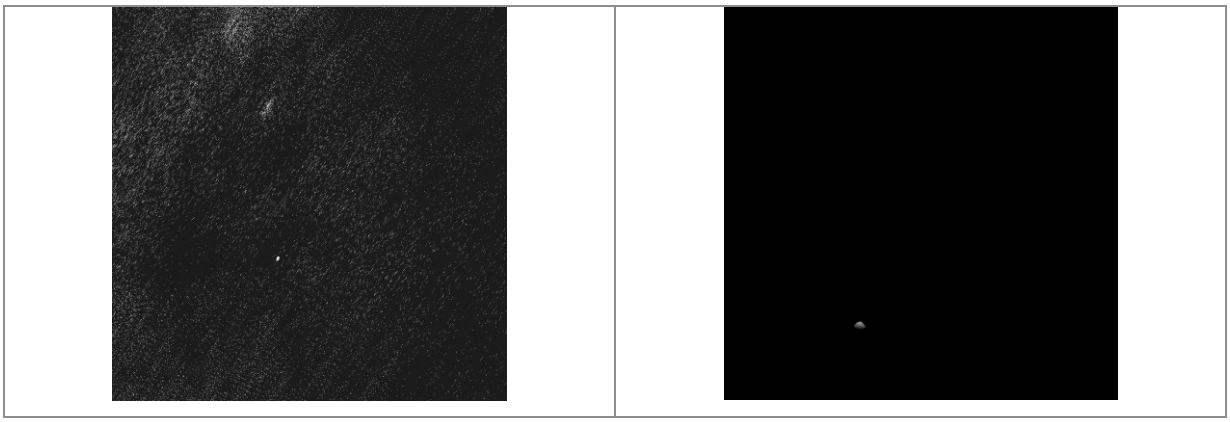


Figure 13. Rendezvous scenario exemplary images generated in PANGU

The lunar landing scenario uses 100 meter resolution DEM model of the Lunar South Pole vicinity. The images from the same trajectory are used for RelNav and AbsNav, with various input frequency (1Hz and 1/10Hz respectively).

Figure 14. Lunar landing scenario PANGU image

The images are fed into the relevant IP algorithms to obtain the IP solution, which is used in the navigation solution to obtain estimated spacecraft position and velocity. The results of the Model-in-the-loop versus Hardware in the loop are presented in section 6.3.

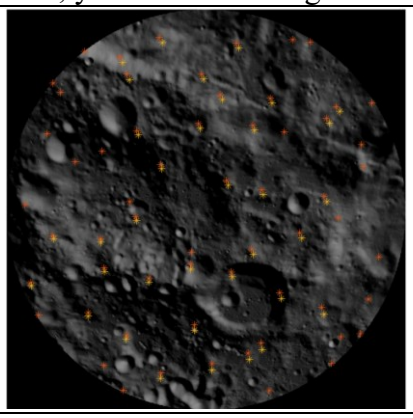
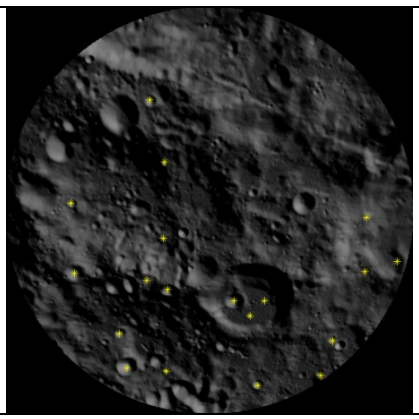
| RelNav tracked features (orange - current image features; yellow – next image features) | AbsNav matched craters |
|---|---|
|  |  |

Figure 15. Lunar landing RelNav and AbsNav IP exemplary image solutions

## 6.2 FPGA in the loop FIL

During the FPGA in the Loop tests, the GMVision system is connected with an external computer by means of SpW interface to a USB brick. This computer provides the test cases input data for the image processing system. The image processing board test execution consists of receiving all the images generated for each scenario and the algorithm execution in the IPB is selected from the FLASH memory available.

After the HW execution, the results obtained from each algorithm is analyzed. The criteria to considerate an accurate detection/tracking is strictly related with the centroiding and feature detections techniques used to compute the detection. A generic representation of the FPGA in the loop test setup is presented into the following image:

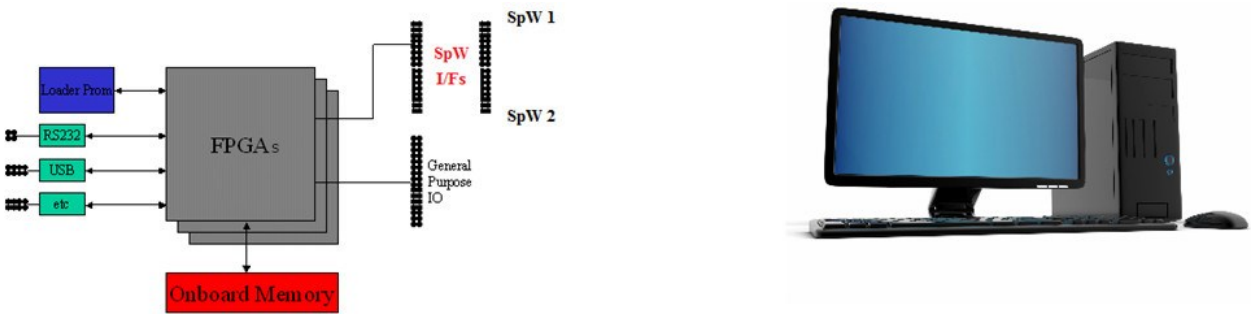



Figure 16. Generic representation of FPGAs in the loop

The HDL implementation is verified extensively using RTL simulation-based verification environments and FPGA-in-the-loop system.

The execution of the FPGA in the loop test bench allow to test the GMVision system with simulated environmental conditions through the dataset of images for each scenario. Each IP is running on the FPGA, the OBC provide to the processing FPGA the PANGU pre-recorded images. In this integration step of the validation, none of the cameras are necessary as the GMVision system is validated and the FPGAs available on the board is simulated with pre-recorded images and the results are compared with the SW results. This validation will verify each image processing IPcore and the interfaces which are space representative (SpW interface). For debugging purposes other interfaces were implemented in order to speed up the implementation such us RS232, CAN, USB. These interfaces were used only during debugging phase but can be added and in future TRL development to be used with different instruments.

## 6.3 Hardware in the loop HIL

During the HIL tests the GMVision system it connected with the LEON3 processor by means of SpW and each camera developed during the activitie [1] and [2] will be as well connected usind the same type of interface. For each scenario the Optical (HIL-OPT) testbench and Dynamc (HIL-DYN) testbench was used to validate the GMVision system.

In order to guarantee the representativeness fo the test results, the images are validated using quality metric and the proper image processing solutions in comparison to the representative SW results. The HIL-OPT testbench set-up using cameras is presented in the following images (Figure 17).

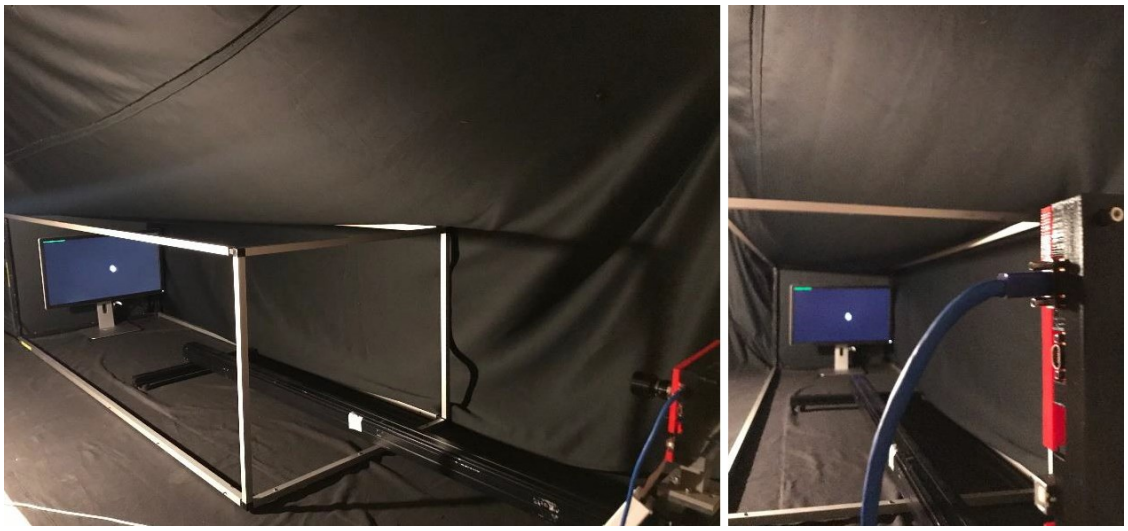


Figure 17. Optical testbench setup

The main goal of the HIL-OPT is to ensure the HW dataflow of the acquired images and the processing of each image for each image processing algorithm. After the validation of the interfaces and the algorithms the tests using the dynamic testbench were performed as described in the following image ( Figure 18), in figure b) and d) the test setup is presented.
The setup is working on a closed-loop and its purpose is to validate the IPB in real-time enviroment.

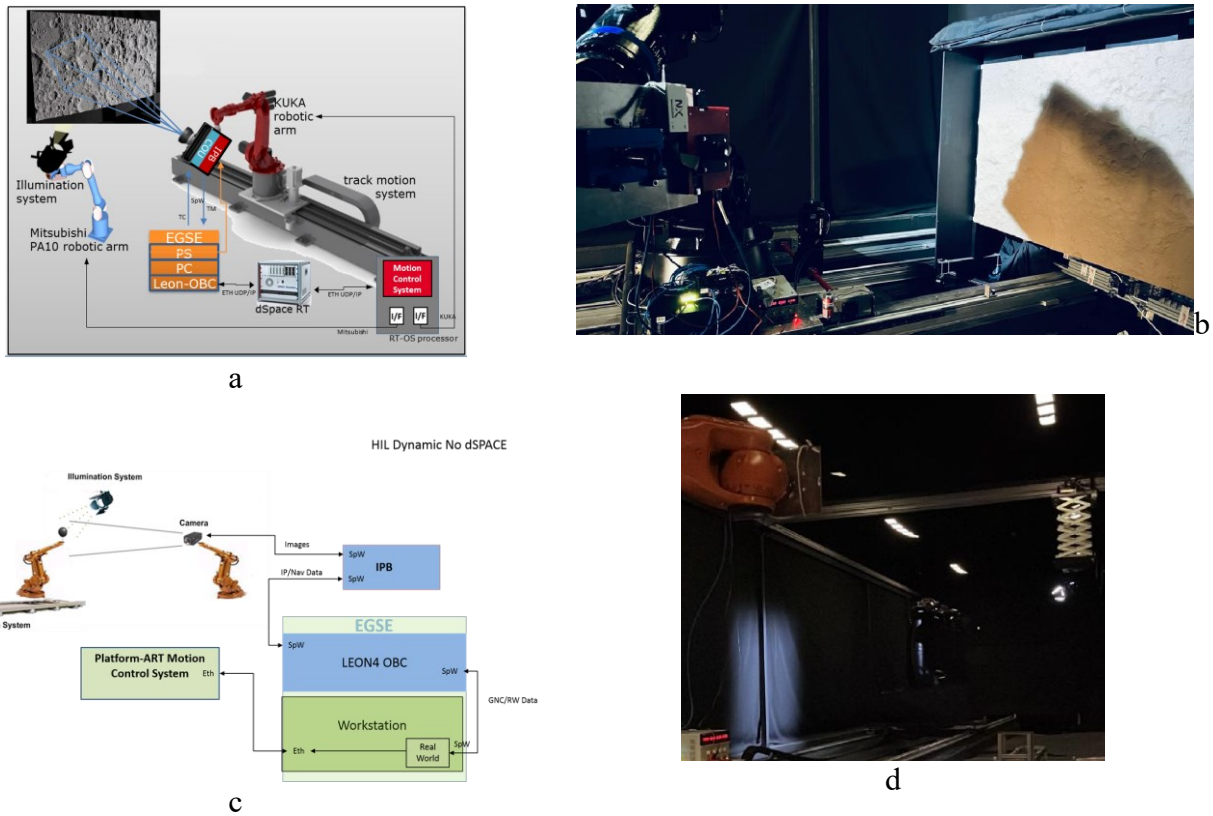



Figure 18. Dynamic test bench proposed, a)&b) Descent end landing scenario, c)&d) rendezvous scenario

The comparison of the SW and HW of each scenario during MIL versus HIL-OPT and HIP-DYN is presented in the following figures.

In Figure 19 and Figure 20, representing rendezvous scenario using FPGA applied IP results, one can notice a small bias in IP from the HIL-OPT tests, being result of imperfect display on the testbench monitor, especially in shadowed

areas of the target. In the HIL-DYN the IP error is slightly dynamic due to capturing the real-world target mock-up in real environment, prone to various noise sources e.g. illumination conditions. However, in all cases navigation errors behave similarly as in MIL tests and the navigation solutions are satisfying.

In Figure 21 and Figure 22 some MIL results worsen towards the end of the scenario, because of illumination in the synthetic images, set to mimic real-world, turning darker when moving towards the south pole, hence the increased error and covariance in some results (e.g. RelNav position altitude). The HIL-DYN over-requirement position errors for the AbsNav scenario are result of the discrepancies with used lunar mock-up in the laboratory. Firstly, the mock-up has never been calibrated with the robotic arm, therefore it was not possible to obtain mock-up ground truth, secondly, mock-up projection from spherical to flat model is not known, which might introduce additional errors on position and attitude, if trajectory projection method was different than mock-up's. One can also notice a late start of the HIL-DYN results, due to limitations of the terrain covered by mock-up. Moreover, due to laboratory limitations, illumination applied was brighter than in synthetic images. Due to these discrepancies, various value of confidence between the MIL and HIL-DYN is put into the measurements, hence diverse covariance in the plots. However, despite the discrepancies, the images captured allowed to obtain navigation results with errors most of the time within requirements, including results from FPGA applied IP for the RelNav MIL scenario.

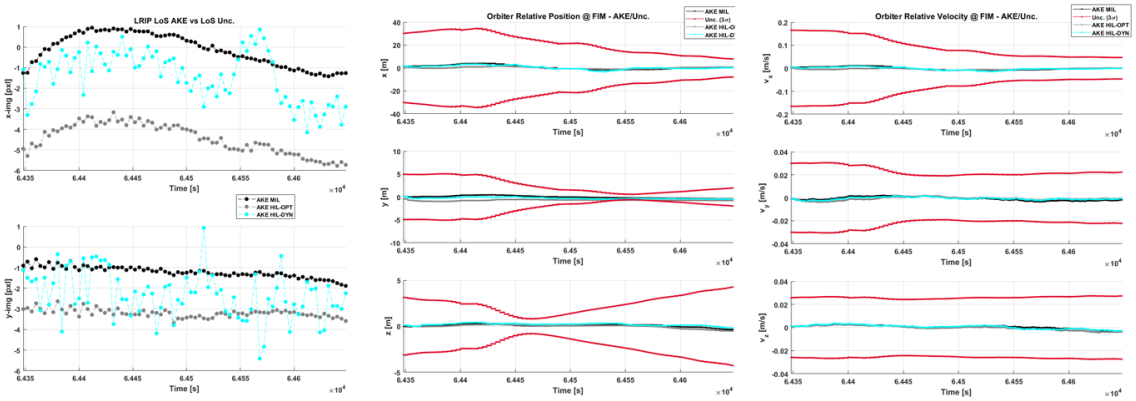



Figure 19. LRIP MIL vs HIL using FPGA IP results. Line-of-Sight AKE; orbiter relative position and velocity AKE

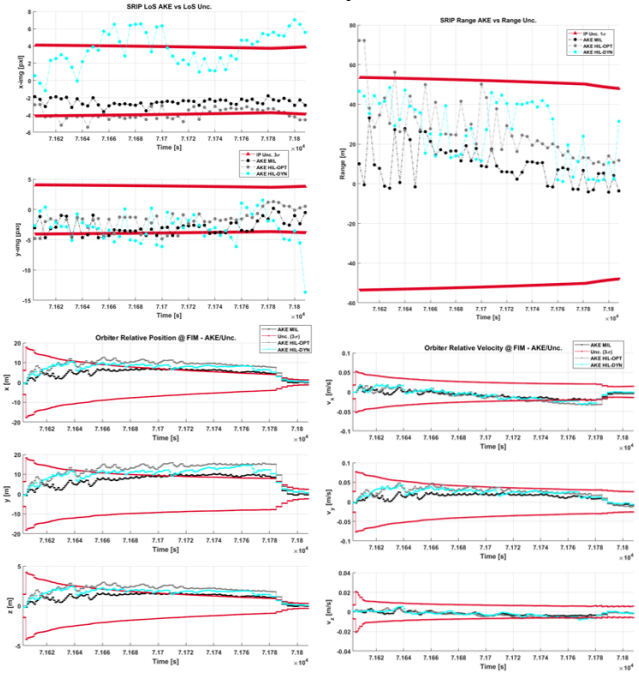



Figure 20. SRIP MIL vs HIL using FPGA IP results. Line-of-Sight, range AKE; orbiter relative position and velocity AKE

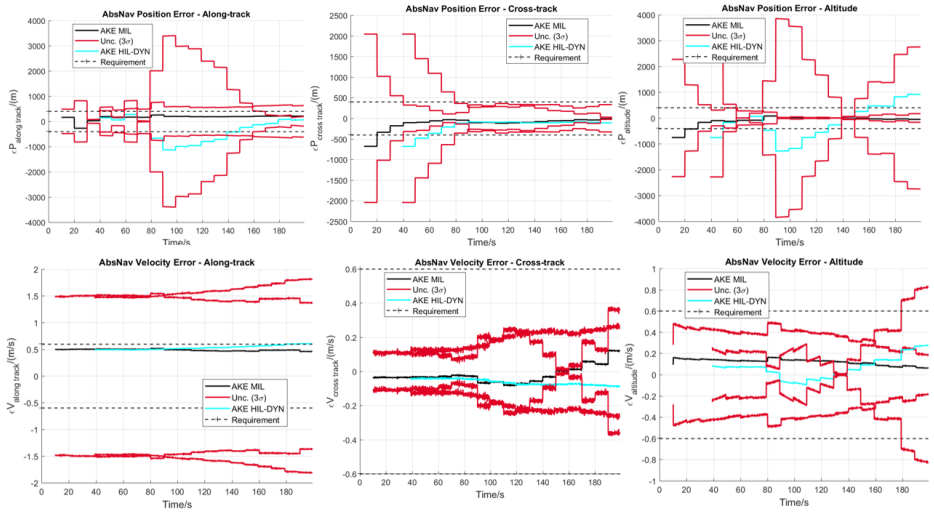



Figure 21. AbsNav MiL vs HIL navigation results. Upper row: position along-track, cross-track, altitude AKE; bottom row: velocity along-track, cross-track, altitude AKE

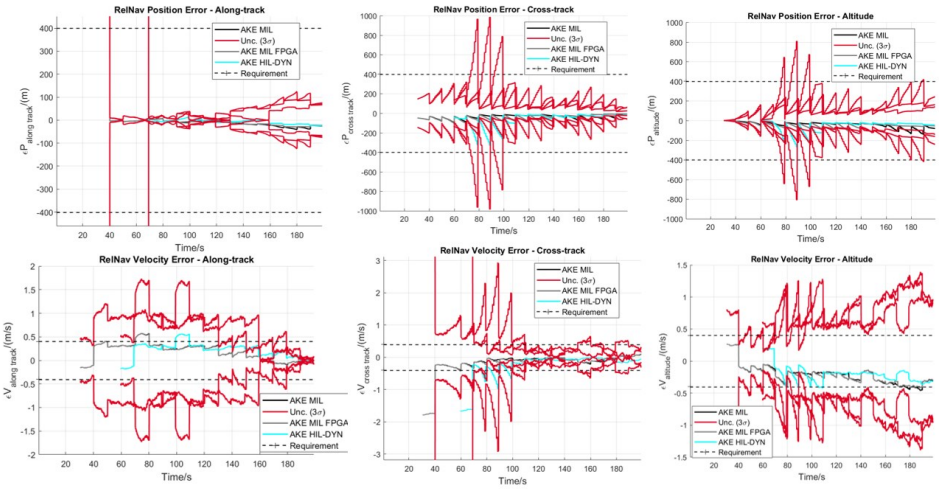



Figure 22. RelNav MiL vs MIL FPGA vs HIL-DYN navigation results. Upper row: position along-track, cross-track, altitude AKE; bottom row: velocity along-track, cross-track, altitude AKE

## 7 CONCLUSIONS

This paper presents an embedded system based on high-performance computer-vision algorithms solution and its implementation deployed in a dedicated HW avionics specifically re-designed in the frame of this work under ESA contract No. 4000132137/20/NL/PA project name GMVision (Image Processing Board Architecture and Co-Processor Upgrade for Vision-Based Navigation)

The re-design purpose was to develop an experimental payload consisting of an independent system which is able to accommodate different image processing algorithms accelerated on-board by a HW implementation based on high-performance rad-hard European FPGAs.

The technical contribution of the presented work incorporates avionics solution concept that achieves a reduced volume and cost-effective architecture. This solution optimally leverages high-performance processing capabilities necessary for on-board algorithms in an autonomous system, while minimizing the impact on the satellite in terms on data processing, power consumption budgets.
This paper presents results for Model-in-the-loop, FPGA- in-the-loop and HW-in-the-loop where there were up to 4 different image processing algorithms implemented and tested inside the avionics.

The TRL to be achieved by the GMVision concept is 6, so the product has not been qualified for flight yet, being built

with commercial components. However, extensive mechanical and thermal analysis was conducted for ambient and space environment. The roadmap towards an actual flight model is deemed with high probability of success, as all the electronics components of the existent EM have space qualified counterparts, so the flight model can be able to withstand the harsh space environment.

The paper presents a highly versatile, fast, and complex avionics development deemed as co-processor for space computer-vision applications. The features, performances, and the evolution of the concept from breadboard model to engineering model, as well as the roadmap towards a powerful flight hardware are presented.

GMVision represents a significant advancement in space-oriented image processing units, meeting the challenges posed by modern space missions. Its integration of advanced image processing algorithms, proven through ESA collaborations, ensures reliable and accurate vision-based navigation. By offering versatility, high performance, compactness, and power optimization, GMVision is poised to enhance the efficiency and success of space missions, supporting autonomous operations and enabling new frontiers in space exploration.

## 8 DISCLAIMER

The work reported in this paper has been performed under a contract of the European Space Agency under the contract ESA Contract No. 4000132137/20/NL/PA known as “Image Processing Board Architecture and Co-Processor Upgrade for Vision-Based Navigation”. The views presented in the paper represent solely the opinion of the authors and should be considered as R&D results not necessarily impacting the present and future system designs.

## 9 REFERENCES

[1] Gonzalez Arjona D., Bajanaru P., Domingo R., Stancu F.A., Alexe A.L., Gogu D.G., Sincan S. “*On-Board Complex Image Processing Based On FPGA Acceleration For Autonomous Navigation In Space*” On-Board Data Processing Conference, European Space Research and Technology Centre, European Space Agency, 2019

[2] Luigi S., Massimo C., Gogu D.G., Bajanaru P., David G.A., Marcos A.R.A., Pesce V., Pellacani A.. *MSR Rendezvous and Capture Phase: the GNC subsystem solution and a snapshot over the Image Processing Algorithms and Narrow Angle Camera elegant breadboard*, 70th International Astronautical Congress 2019

[3] A. Bidaux-Sokolowski P. Kicman, M. Klaka, Laura Mujdjei, Dragos Georgel Gogu , Francesco Cocco , Finn Ankersen , Camille Piratd, Roger Walkerd. *GNC design for Rendezvous Autonomous CubeSats Experiment (RACE) Mission*, 11th International ESA Conference on Guidance, Navigation & Control Systems 22 - 25 June 2021, Virtual and 8th ICATT (International Conference on Astrodynamics Tools and Techniques) 23 - 25 June 2021, Virtual

[4] Stancu F.A., Moreno Villa V. M., Dominguez Sanchez C., Plămădeală A. V., Ovejero Provencio D, *Visual based GNC system from prototype to flight software*, INCAS Bulletin, Vol. 15, Issue 1, 97 – 106, 2023

[5] Stancu F.A., Garcia J. R., Pellacani A., Gonzalez Arjona D., *Validation process from models to HW avionics in the frame of HERA navigation*, Dasia (Data system in aerospace), 2023.

[6] *System Design and Performance Evaluation of Advanced Optical Terrain Absolute Navigation for Pinpoint Lunar Landing*, Marcos Avilés Rodrigálvarez, Marco Mammarella, Ana María Sánchez Montero, Pablo Colmenarejo Matellano, 8th International ESA conference of Guidance, Navigation & Control System

[7] *Comparison of Optical Terrain Absolute Navigation Techniques for Pinpoint Lunar Landing*, Marco Mammarella, Marcos Avilés Rodrigálvarez, Ana María Sánchez Montero, Bach Van Pham, Simon Lacroix, 62nd International Astronautical Congress.