

CMOS Image Sensor camera electronics for solar science instruments

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ABSTRACT

Modern CMOS Image Sensors (CIS) offer an alternative technology to traditional Charge Coupled Devices (CCDs) for upcoming solar science instruments. Their key advantage is the integration of many parallel pixel readout and digitisation chains within the device, permitting higher frame rates and lower overall camera complexity by removing the need to implement this process externally. Higher frame rates promise to enable better cosmic ray rejection in output data and frame stacking techniques that can meet or exceed the saturation signal, particularly relevant for solar science applications, and noise performance of current CCD cameras.

Building on extensive experience with CCD based cameras, and in response to upcoming opportunities, the authors have developed a flight-ready camera electronics unit capable of operating at these higher frame rates and conducted a partial qualification campaign intended to raise the design to TRL 6. The camera inherits much of its design from existing RAL Space CCD camera electronics. However, there are some key changes, the camera takes a 100 mm by 100 mm by 40 mm form factor, with no enclosure for ease of mechanical integration; and makes use of a SpaceFibre communications link to enable the output data rates required for high frame rate operation. While the current design uses a Teledyne e2v CIS120 XLS variant for its large per-pixel full well capacity other interface compatible image sensor variants offer lower noise performance and provision has been made to accommodate fully depleted image sensors.

The justification and design of the camera electronics are presented, alongside initial performance measurements and the preliminary results of a thermal vacuum (TVAC) environmental test campaign. This includes: modelling demonstrating possible applications of the CIS camera as a drop in replacement for existing CCD cameras; an outline of the design elements and key changes in the electronic design from previous CCD cameras; measurement of the noise, saturation signal, and power consumption values for the camera; and the variations of these parameters observed during TVAC testing.

Keywords: CMOS Image Sensor, Readout Electronics,

1 INTRODUCTION

A set of camera electronics have been developed at RAL in response to upcoming opportunities for CMOS Image Sensor (CIS) based solar instrumentation and a partial qualification campaign conducted with the intention to raise the design to TRL-6. Due to the function of this system, and its unusual mechanical design when compared to previous RAL projects, the camera electronics have been named: CIS ReadOut, Without enclosure (CROW). In this paper, an expected use case for a CROW-like camera will be explored, the CROW itself will be detailed, and the results of performance and environmental testing will be presented.

2 CIS APPLICATIONS IN SOLAR PHYSICS

CIS detectors have now been adopted by multiple solar science instruments [1], [2], with particular attention paid to their increased radiation hardness when compared to charge coupled devices (CCDs), alongside possible power benefits. Further adoption can face barriers due to a lack of heritage, or unfavourable performance comparisons to traditional CCDs. When

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compared to a CCD, CIS can be limited by larger pixel to pixel non-uniformity and a dynamic range and full well capacity (FWC) limited by the voltage range available to the pixel and readout circuits on a CMOS chip.

However, current space qualified CIS detectors may be able to meet and, under certain conditions, exceed the performance of traditional CCDs by leveraging their highly parallelised architecture to achieve greater framerates. This is particularly true for applications such as solar coronagraphy in which the dominant form of detector noise is photon shot noise, counteracted by accumulating the greatest possible signal. By simply stacking more frames for a single exposure a CIS can emulate the greater full well capacities of a CCD. Performance in this application depends on the total detector noise exhibited in the frame stack, as expressed in equation 1.

$$\sigma_{pix} = \sqrt{\mu_{sig} + n\sigma_{readout}^2 + \mu_{dc} + n\sigma_{quant}^2}. \quad (1)$$

Where σ_{pix} is the rms noise of the signal measurement in a single pixel; μ_{sig} is the mean photon signal during the exposure (contributing shot noise); μ_{dc} is the mean dark current (also contributing shot noise); n is the number of stacked frames; $\sigma_{readout}$ is the readout noise (therefore $n\sigma_{readout}$ is the total readout noise in a stack of frames); and $\sigma_{quant.}$ is the quantisation noise in each pixel measurement (equal to the analog to digital converter (ADC) quantisation value divided by $\sqrt{12}$).

Equation 1 indicates that for large values of μ_{sig} , the readout and quantisation noise (multiplied by the number of stacked frames) can be quite large before they appreciably impact the total noise of the detector. In order to demonstrate how this relates to the use of a lower full well CIS, incurring extra noise due to frame stacking, the performance parameters of the CROW and a roughly equivalent CCD camera (developed for PUNCH) were used to model noise, and therefore SNR performance, for a range of signal values. The minimum image cadence of the PUNCH camera is 2.5 s (0.4 fps); to match its FWC, the CROW must stack four frames with a framerate of 1.6 fps to produce a frame stack at an equivalent rate. This is well within the capabilities of the CROW hardware. The parameters of the respective cameras have been recorded in Table 1, while the resulting noise and signal to noise ratio (SNR) values have been plotted in Figure 1 (it has been assumed that the image sensor in each camera has been cooled until dark current is negligible).

The SNR advantage of the PUNCH camera over the CROW has been plotted as the last pane of Figure 1. While the advantage of the CCD is undeniable at very low signal levels, this advantage has reduced by the time the signal has reached a few thousand photons.

Table 1. Noise parameters used for performance comparison.

Value	Unit	PUNCH [3]	CROW (<i>this work</i>)
$\sigma_{readout}$	e ⁻ rms	18	16
FWC (linear)	ke ⁻	300	85
ADC bit depth	bits	16	12
$\sigma_{quant.}$	e ⁻ rms	1.3	6.0
n	frames	1	4
$\sigma_{pix, \mu_{sig}=0}$	e ⁻ rms	18	34

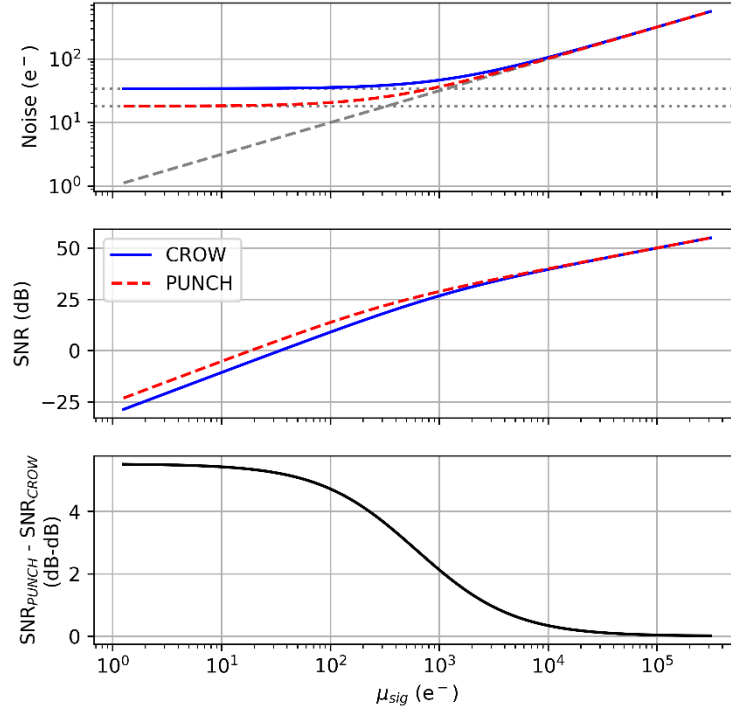


Figure 1. Noise, SNR and SNR advantage expected of a PUNCH-style and CROW-style camera system. At high signal levels the noise of both systems is dominated by shot noise on the incoming photons. At lower signal levels the PUNCH-style camera exhibits better noise performance.

To contextualise these values, the signal profile derived for the SCOPE coronagraph [4], [5] and improved straylight model [6] were used to derive the expected performance of the PUNCH and CROW camera electronics for that application. The SCOPE coronagraph was intended to observe Coronal Mass Ejections (CMEs) by observing the solar corona from 2.7 solar radii to 25 solar radii. Design effort for such an instrument is focussed on blocking light from the solar disk and suppressing the associated diffraction and straylight. This is an ideal application for a CIS camera such as CROW: instrument noise performance is dominated by the presence of large interfering signals including other coronal structures and straylight, with corresponding photon shot noise, as opposed to the noise of the detector.

Shown in Figure 2, the SNR of the entire useful science signal expected for this instrument is photon shot noise limited. This means that, even though the predicted noise performance of the CROW is worse than the PUNCH model, it does not impact the expected instrument noise performance. SCOPE was designed to operate with 2x2 pixel binning and three frames stacked per image while using a PUNCH-like camera. This binning and stacking have been retained and modelled for the CROW, in addition to the frame stacking used by the previous example.

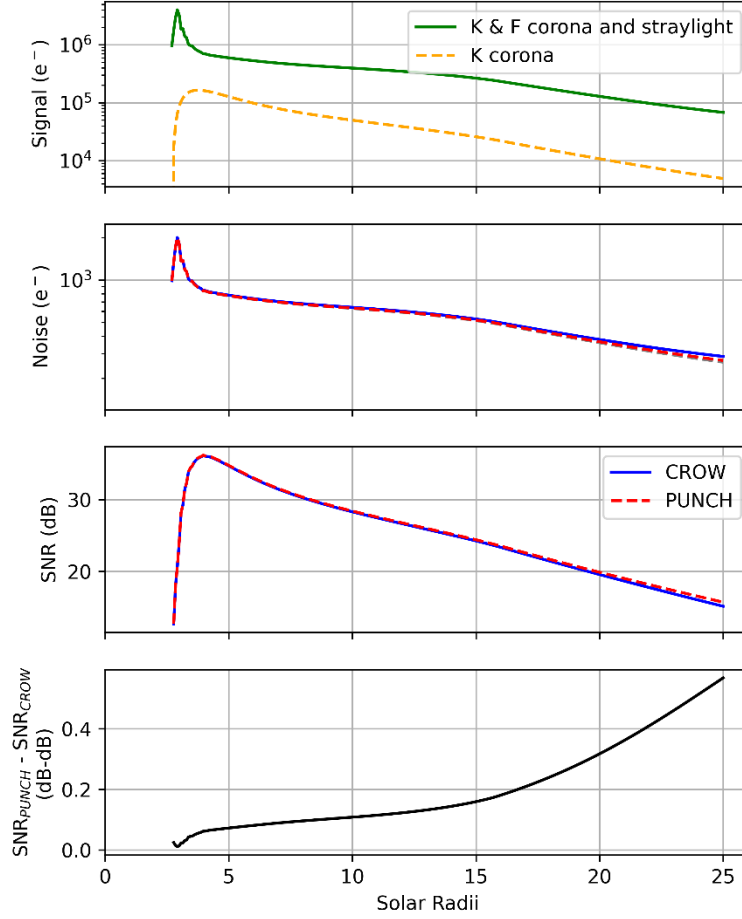


Figure 2. SCOPE/COR signal model and corresponding noise and SNR models. SNR has been measured relative to the K corona signal.

While this analysis has assumed that the CROW would be operated to mimic the PUNCH camera noise performance, CROW can detect far larger signals by taking the stacked frame method further. Taken to the extreme, at its full framerate of 10 fps the CROW could measure signals up to $1 \times 10^6 \text{ e}^- \text{ s}^{-1}$. It may also be preferable to minimise the CIS integration time to reduce the number of cosmic ray interactions in each image, reducing contamination of any downstream data-pipeline.

As demonstrated in Figure 1, frame stacking has limited performance for lower signal levels, largely because the multiple exposures repeatedly incur readout noise in the measurement. Other methods of high dynamic range (HDR) imaging are expected to be possible in upcoming space-qualified CIS detectors including switched capacitor (dual-gain) and up-the-slope imaging [7]. These HDR methods reduce the number of times a pixel is read out for a single measurement, reducing the readout noise penalty and are therefore expected to offer CCD-like scene dynamic range while also comparing favourably with the saturation signal and detector noise performance achievable with a CCD.

3 CAMERA DESIGN

The CROW to incorporate experience derived from previous RAL CCD cameras, permitting rapid design, production, and qualification of a system that makes use of space-qualified parts. It has been built to operate a single CIS120 image sensor [8], the extra-large signal variant of this device has been used during development. It is implemented on a single flex-rigid printed circuit board (PCB) intended to be folded for ease of integration into larger instruments. It includes

several features intended to allow the CROW to fulfil the requirements of an instrument wanting to exploit the full performance of the CIS detector. These include:

- Use of a high-speed output data link to permit full-frame data output while operating the CIS at its maximum framerate.
- Use of an RTG4 field programmable gate array (FPGA). While no image processing is currently implemented, resource availability in the FPGA means complex tasks on CIS data may be performed as it is passed through the FEE if required.
- The CIS is mounted at the end of a long length of flex PCB, permitting the CIS and the rest of the electronics to be mechanically isolated from each other for instruments with stricter optical bench requirements.

During design, several different high speed output data link solutions were considered. However, SpaceFibre was preferred as a developing industry standard for high bandwidth data transfer, its low harness mass, and large potential throughput.

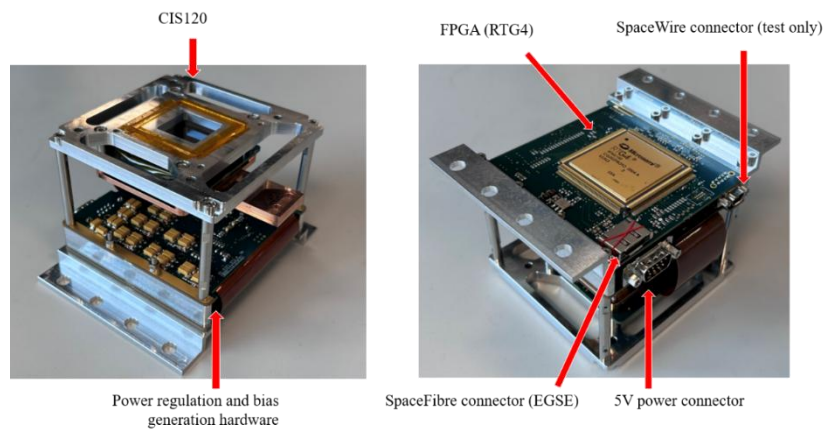


Figure 3. CROW mounted in environmental qualification test fixtures, with its key elements indicated.

Functionally, the CROW is very similar to existing CCD front end electronics designs [3], [9]: CIS control, sequencing and readout functions are performed with an FPGA which also operates a set of bias control and housekeeping monitoring circuits. Communication with a payload or spacecraft controller is achieved with a single data link which carries commands, telemetry, and image data. The camera system block diagram is shown in Figure 4.

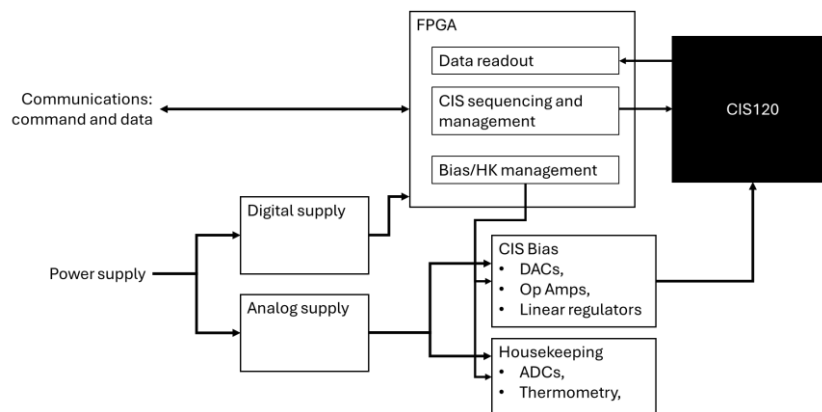


Figure 4. CROW system block diagram.

This development has also drawn heavily on the results of experiments conducted on an earlier development testbench for the CIS120 image sensor. Testing was conducted with the power supply and bias architecture for the CIS. This included measuring image sensor noise performance for power and bias configurations with a minimal number of regulators and

injecting noise directly into supplies and biases. In each test the CIS and camera electronics combination demonstrated remarkable resilience, with no impact on electro-optical performance parameters observed. Therefore one key innovation permitting the compact implementation of the CROW is the use of the RAL DAC MK3 application specific integrated circuit (ASIC) [10] for direct generation of CIS voltage biases, without the use of additional op amps used for final stage noise isolation of the image sensor.

Table 2. CROW design parameters.

	Unit	Value	Notes
Image sensor		CIS120 XLS	Electronics compatible with other CIS120 variants. Camera performance is detector limited.
Output data rate	Gbps	~1.6	Higher rates possible, link speed chosen to accommodate 10 fps data
Width	mm	100	
Length	mm	100	
Height	mm	50 - 76	Dependent on use of CIS segment flex

4 PERFORMANCE MEASUREMENTS

Initial performance testing of the CROW has been performed under ambient lab conditions during commissioning of the camera hardware at 3 fps, prior to the completion of digital design work required for 10 fps operation. While some change in noise performance may occur once the full framerate has been achieved, these measurements are representative for slower operation of the CROW (including the hypothetical application of section 2), and indicative for full framerate operation. An electro-optical test campaign was conducted to measure the parameters of particular interest for the camera design.

Electro-optical measurements were made using the test setup shown in shown in Figure 5. A light emitting diode (LED) driven by a microcontroller was used to provide illumination to the image sensor through a diffusion screen. The diffusion screen, spacing between the screen and image sensor, and tilting the LED to mitigate its directivity were used to ensure a moderately flat field illumination for testing. The illumination of the image sensor was controlled by varying the pulse width modulation (PWM) duty cycle used to drive the LED.

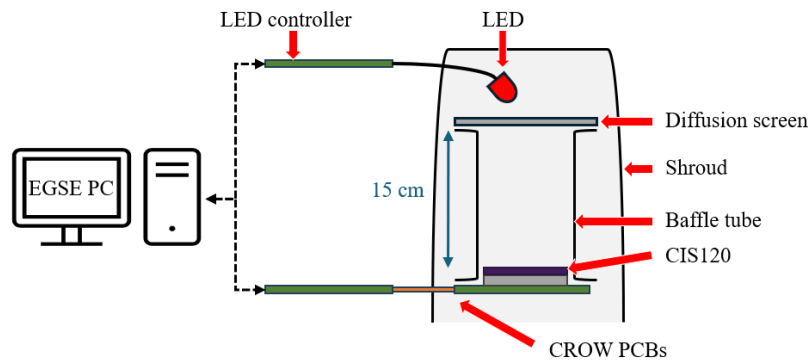


Figure 5. Diagram of test set up for performance measurements of CROW.

Figure 6 shows a PTC measured with the CROW, used to derive a conversion gain. To mitigate any non-uniformities in illumination, a region of interest (ROI) was used to perform this measurement, selected by identifying a region of flat illumination from data with moderate illumination signal. The PTC data is plotted again in Figure 7, though with the mean

signal of the ROI and PWM duty factor of the LED, which is assumed to map linearly to the illumination produced by the LED.

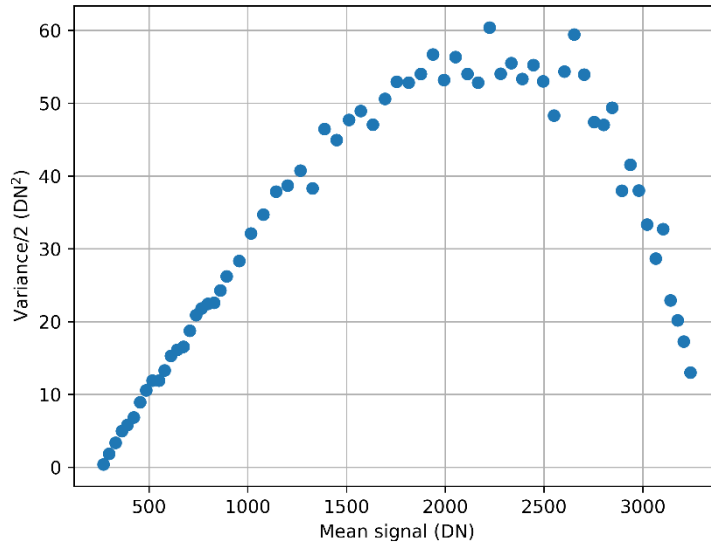


Figure 6. CROW photon transfer curve measured under ambient conditions.

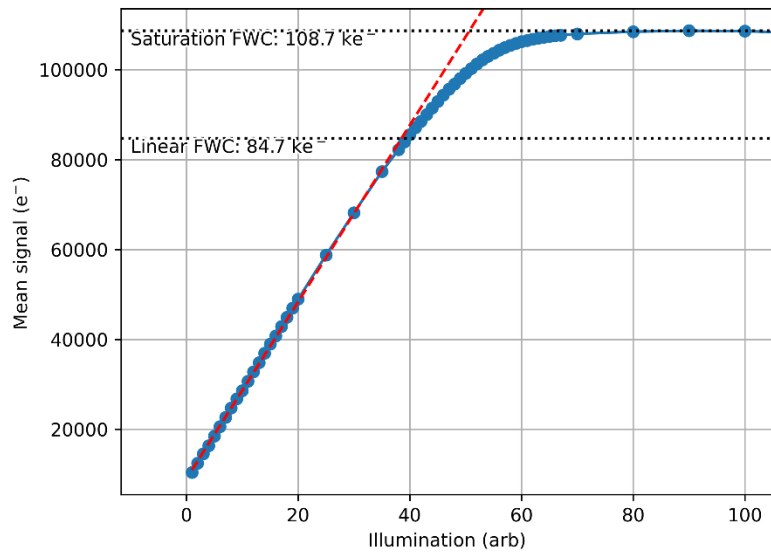


Figure 7. CROW linearity measurement measured under ambient conditions.

Dark current and readout noise were measured with dark frames taken with varying integration times. Figure 8 and Figure 9 report the recorded values, as well as a histogram of the pixel population for both parameters. Raw dark current measurements taken under these conditions are prone to error due to the uncontrolled temperature of the CIS. While the CROW includes provision for thermal control of the CIS via a cold strap, the CIS was left thermally isolated for these tests. At the conclusion of testing the CIS temperature was measured to be 30 °C, which has resulted in an increase in the average dark current measured. The increase is consistent with a 7 °C doubling temperature and the datasheet dark current value.

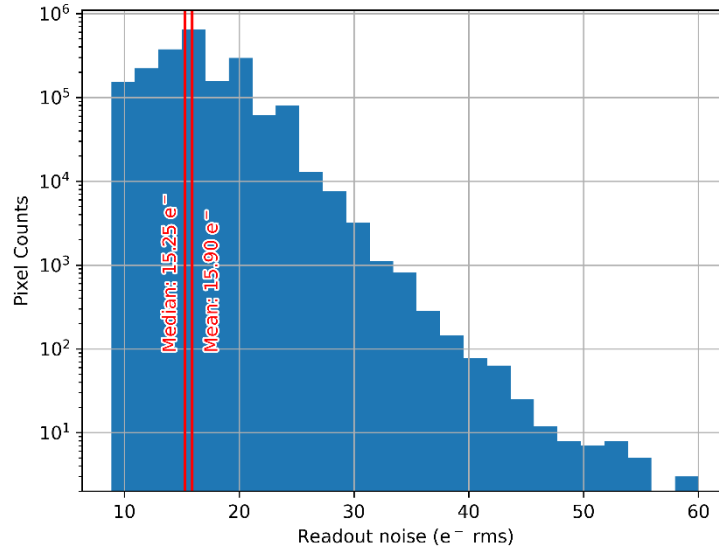


Figure 8. CROW per-pixel readout noise histogram measured under ambient conditions.

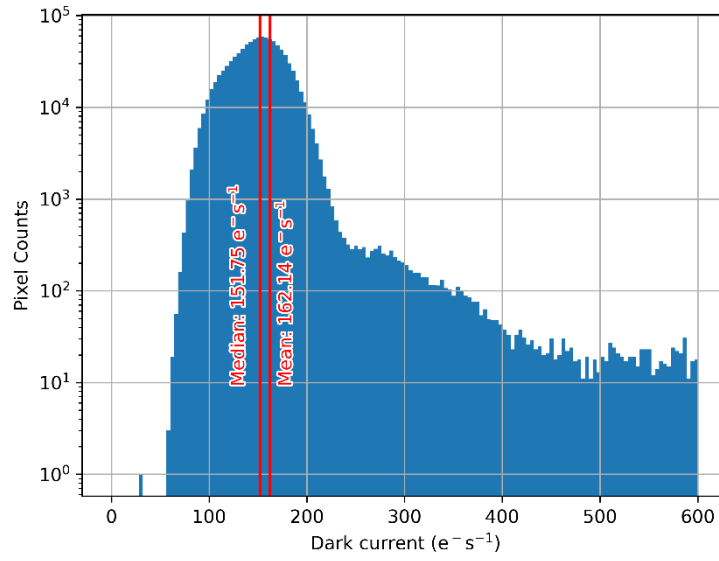


Figure 9. CROW per-pixel dark current histogram measured under ambient conditions.

Finally, during testing the current drawn by the hardware was observed. The electronics were observed to draw 750 mA of current while idle, and 850 mA of current while imaging, from the input 5 V power supply. All measured performance values (summarised in Table 3) are well within the range expected of the CIS120 XLS image sensor [11].

Table 3. Measured performance parameters of the CROW operating a CIS120 under ambient lab conditions.

Parameter	Unit	Value	Note
Conversion gain	$e^- \text{ DN}^{-1}$	31.1	
Readout noise	$e^- \text{ rms}$	16	
Dark current	$e^- \text{ s}^{-1}$	162	Ambient temperature and pressure
Pixel FWC (linear)	ke^-	84.7	To 1 % linearity
Pixel FWC (saturation)	ke^-	109	
Power	W	4.25	Ambient temperature and pressure
Power (Idle)	W	3.75	Ambient temperature and pressure

These tests have demonstrated that the CROW can operate CIS120 XLS image sensors with detector limited noise and FWC performance and will provide a performance baseline for subsequent environmental testing of the hardware. An example scene in the lab was used for final demonstration of the CROW's function, shown in Figure 10.

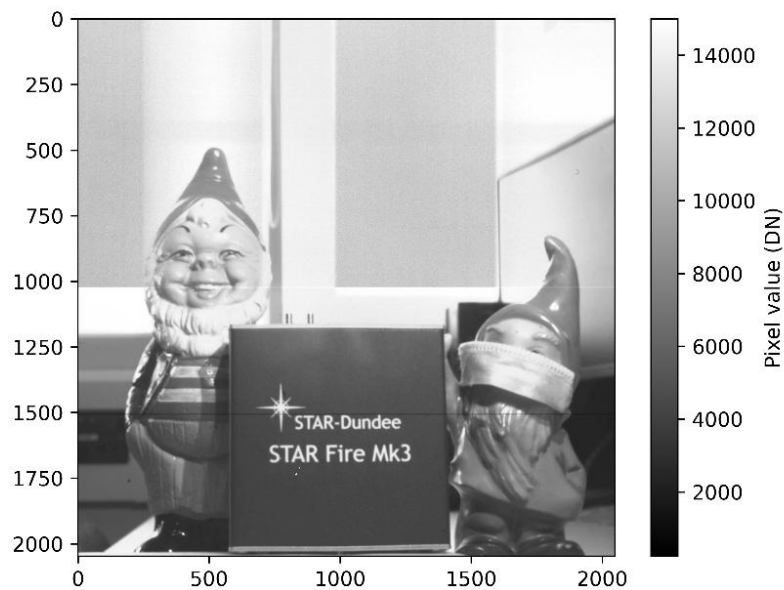
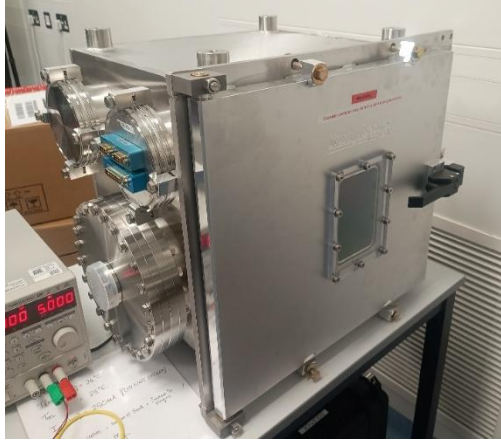


Figure 10. Demonstration scene observed with the CROW.

5 INITIAL ENVIRONMENTAL TESTING RESULTS

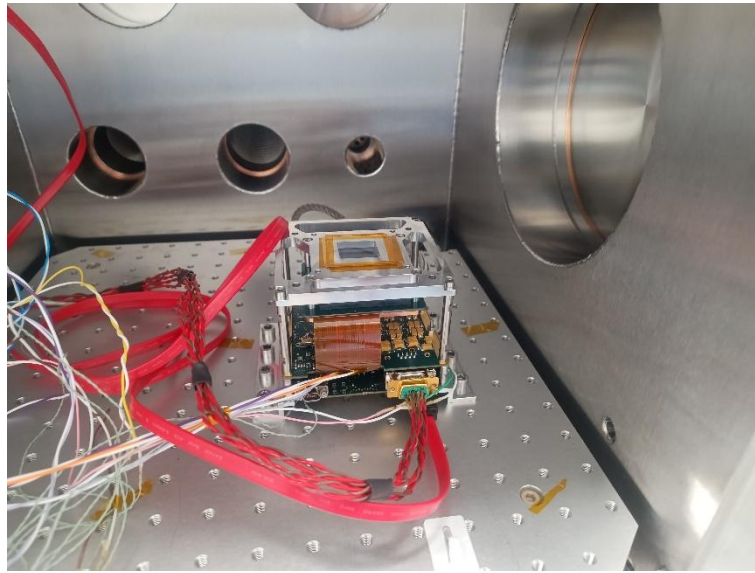
Development of the CROW has included environmental qualification across a nominal operational and non-operational temperature range. This has made use of a board-level thermal vacuum (TVAC) test chamber, shown in Figure 11.



(a)



(b)



(c)

Figure 11. (a) Test apparatus used for environmental qualification of the CROW, (b) installation in progress, and (c) the CROW installed in the vacuum chamber.

While full qualification testing is ongoing, preliminary testing results have demonstrated operation of the CROW hardware at a representative instrument maximum operating temperature. Modelling of the CROW system during design indicated that the primary component consuming energy in the camera is the RTG4 FPGA, and its associated power regulation components, a chain of three linear regulators used to provide the core logic voltage of 1.2 V from the input power. Together these four components are expected to represent 60 % of the power consumption of the camera. Manufacturer information indicates that FPGA core logic current consumption increases with temperature [12] (shown in Figure 12) which is expected accentuate the effect of any increase in interface temperature and be the limiting factor for the hardware's maximum operating temperature.

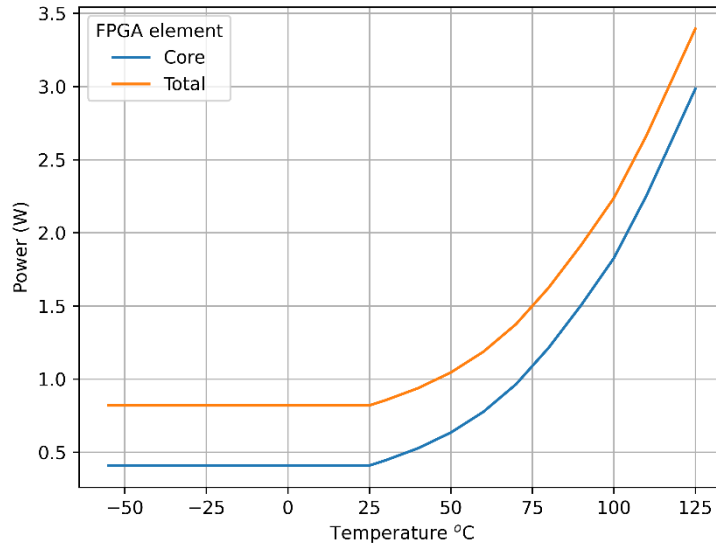


Figure 12. FPGA power consumption prediction for junction temperature during FPGA design.

Prior to conducting any tests thermal modelling was used to predict component junction temperatures across the range of temperatures to be tested, with a particular focus on the upper end. This modelling used manufacturer thermal resistance values for the regulator and FPGA components (junction to PCB resistances of $23.2 \text{ }^{\circ}\text{C W}^{-1}$ for the linear regulators, and $0.26 \text{ }^{\circ}\text{C W}^{-1}$ for the FPGA) and equations 2 to 6 which relate the input and output currents and voltages of each component to the dissipated power.

$$I_{out,1.2V} = I_{in,FPGA,1.2V} \quad (2)$$

$$I_{out,n} = I_{in,FPGA,n} + I_{out,n-1} + I_{q,n-1} \quad (3)$$

$$P_{diss,n} = (V_{in,n} - V_{out,n})I_{out,n} + V_{in,n}I_q \quad (4)$$

$$P_{diss,FPGA} = \sum I_{in}V_{in} \quad (5)$$

$$T_{component} = T_{PCB} + P_{diss}R_{th,JP} \quad (6)$$

Where $I_{in,n}$ and $I_{out,n}$, and $V_{in,n}$ and $V_{out,n}$ are the input and output currents and voltages for the n^{th} linear regulator (the 1.2 V regulator being regulator $n = 0$); $I_{in,FPGA,n}$ is the current drawn by the FPGA from the output of the n^{th} linear regulator. P_{diss} is the power dissipated in a component; $T_{component}$ is the junction temperature of a component; T_{PCB} is the temperature of the camera PCB; and $R_{th,JP}$ is the junction to PCB thermal resistance of a component. The quiescent power draw of each linear regulator, I_q , has been modelled but is not the dominant driver of power dissipation.

The modelling indicated that a nominal system maximum operational temperature (of $50 \text{ }^{\circ}\text{C}$) will result in junction temperatures of $54 \text{ }^{\circ}\text{C}$ for the FPGA, and between $75 \text{ }^{\circ}\text{C}$ and $83 \text{ }^{\circ}\text{C}$ for the linear regulators, which are well within the maximum operating temperatures of these components.

To verify that the CROW hardware was able to complete the full qualification campaign an initial temperature sweep up to the maximum operating temperature has been completed. During this early commissioning phase only the final 1.2 V output linear regulator and FPGA could be monitored. The sweep was conducted incrementally, with results from each

step checked before proceeding to ensure that no components were likely to inadvertently exceed their maximum operating temperatures. The results are shown in Figure 13.

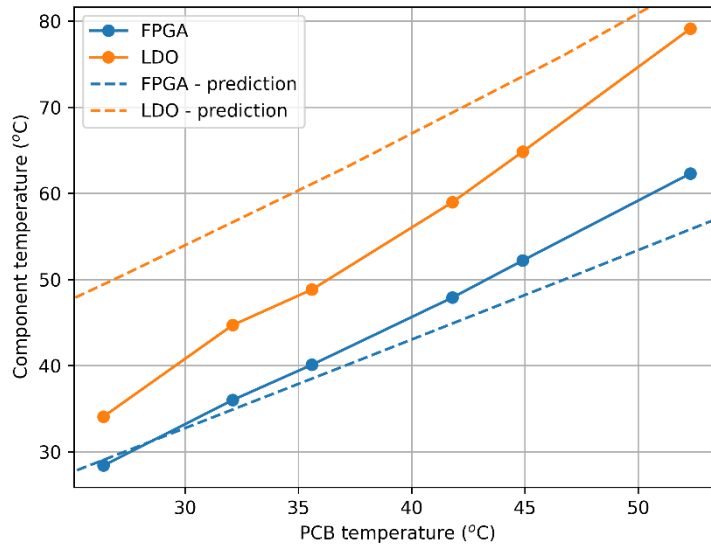


Figure 13. Recorded FPGA, PCB, and linear regulator (LDO) temperatures recorded during initial speed of the CROW hardware prior to completion of the qualification campaign.

These results indicate that the thermal model used to predict the component temperatures require refinement. Conversely it has also demonstrated operation of the CROW at a typical instrument maximum operating temperature. Qualification testing is ongoing and will result in improved thermal modelling of the hardware, possibly permitting the acceptable operating temperature range of the CROW to be extended.

6 CONCLUSIONS

Continuing advancement of CIS technology presents opportunities for new solar instrument designs. The CROW hardware has been developed in response to early opportunities for such instruments. Performance testing of the hardware has indicated the readout electronics exhibit detector-limited electro-optical behaviour. The hardware is completing a thermal qualification campaign, to levels derived from previously developed solar instruments, and is now being investigated as a candidate for use by in-development instruments.

Lessons learned during design and test of the CROW have fed into ongoing readout electronics development. Success of the DAC Mk3 ASIC as a stand-alone bias generator has prompted further investigation of potential future ASIC developments at RAL. This would combine the DAC Mk3 design with additional current bias generators and telemetry circuits to reduce the number of additional components required by the camera to further reduce the size and power consumption of the system.

To date the CROW has been tested with an ‘extra-large signal’ variant CIS120. However, other versions of this device are compatible with the design with the potential to offer lower noise, higher framerates, or deep depletion for instruments as required. Investigation of the CROW’s performance with these detectors is a potential avenue for further study.

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