multiMIND – High Performance Processing System for Robust NewSpace Payloads

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Challenge | Motivation

/// COTS processors, MPSoC, AI accelerators offer high computation power

- Not designed for space, but: enables things not possible before
- Space grade alternatives do not exist or are not an alternative in terms of SWaP
- Caution! Higher risk! Has to be compatible with mission needs.
- We have to face some compromizes (mainly availability)

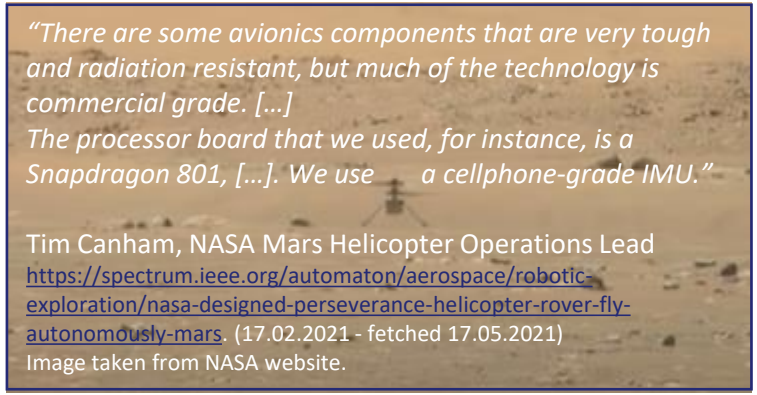
/// New missions benefit from onboard (pre-)processing

- Enables missions and operations not possible before
  - Ingenuity: would never fly with >2x mass / >2x power
  - COTS SAR (Iceye) not feasible with COTS in this SWaP
- **Onboard processing linke on ground**
- Its not only the processing hardware: Many processing steps require use of S/W and F/W building blocks, which were:
  - … never designed for space use
  - … not compliant to coding rules
  - … not really reviewable due to their sheer size

  Software (O/S, drivers, libraries etc.) needs to be considered as well.

  fast time-to-market due to reuse of standard tools commonly used by a big market - no single-purpose developments

  Note: In some applications, development of S/W costs more than development of H/W.



"There are some avionics components that are very tough and radiation resistant, but much of the technology is commercial grade. […]
The processor board that we used, for instance, is a Snapdragon 801, […]. We use a cellphone-grade IMU."

Tim Canham, NASA Mars Helicopter Operations Lead
https://spectrum.ieee.org/automaton/aerospace/robotic-exploration/nasa-designed-perseverance-helicopter-rover-fly-autonomously-mars. (17.02.2021 - fetched 17.05.2021)
Image taken from NASA website.

Target is non mission-critical applications or missions, where some risk of unavailability is acceptable (e.g., constellations with a high number of satellites or short lifetime and easy replenishment).

Intended orbit: LEO < 1000 km
Mission duration: 3 to 8 years

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Comparison of processing engines / MPSoC candidates

/// FPGA | Processor or MPSoC

- MPSoC combines efficiently FPGA + Processor in one chip
- FPGA off-loading gains >10x compared to processor alone
- Hard-block processor in MPSoC runs >3x faster than soft-core in FPGA
- However: This applies for calculation demanding applications where good FPGA / processor workshare is possible. Especially signal, video or SAR processing!

/// Evolution Zynq 7000 → Ultrascale+

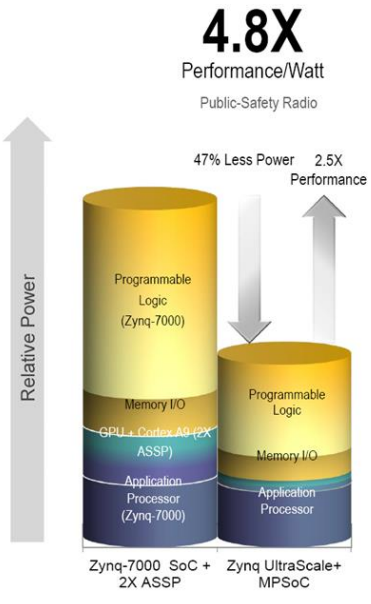
- Number of DSP 2x to 10x
- Power efficienty > 4x
- Fabric increase > 2x
- Radiation effects:
  - Processor cores seem more robust (SEFI less frequently)
  - SEU mitigation improved (memory bits scrambled; cache ECC, triplicated PMU, CMU)
  - SEL observed (non-destructive when properly mitigated)

/// Alternatives

- NanoXplore large / ultra:
  - NX large is too small
  - NX ultra not yet available; also smaller than Ultrascale+
- Intel MPSoC
  - Potentially interesting candidates
- Other MPSoC or integrated systems
  - Interesting candidates, but:
  - Less knowledge and heritage available
  - Possible as separate co-processors / companions

For the selected mission and application profile, the Xilinx Zynq Ultrascale+ series is used. However, specific mitigation strategies against SEL is required.

Application Example – AIS receiver



source: Xilinx

/// Evolution required from Z7000 series to next generation

Many SDR applications are limited by MPSoC performance onboard!

/// Example: AIS receiver with multi-beam antenna management

Receiver with multi-Doppler correlator for beam-forming / degarbling
Note: this application is representative for a multitude of IoT systems and the challenges there.
Similar results were obtained for ADS-B decoding payloads.

Item	State-of-the-art solution (Z7030 based)	Proposed new solution (Ultrascale+ ZU6EG)	Remark
# channels	2 with correlators	4 with correlators	Twice the channels
# correlators	Limited Doppler processing	Full Doppler processing (2x correlators of Z7030 design)	More ressources available per channel, allowing better degarbling / separation
Message decoding	Limited by dual core A9	4x capacity of Z7030 variant	4 times message throughput
Power consumption (relative)	**Payload based on Ultrascale+ requires roughly half the power per processed message compared to Z7030**		

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Applications and Challenges for Advanced Nanosat Payloads

/// IoT systems

- Require high amount of processing:
  - Massive amount of messages, usually no media access protocol
  - Highly agile overlapping scenario
  - Deconflicting algorithms demant high processing power
- Usually on-board processing power limit capacity of the system, not the spectrum capacity!

/// EO systems

- EO systems benefit from on-board processing
  - Data reduction
  - Scouting (pre-selection of interesting areas)
  - Onboard classification
- Massive on-board processing
  - High speed interface to digitizers
  - Aggressive data reduction (compression, EO based classification, demodulation)

/// General challenges

- Many systems operate in environments not fully characterized at launch
  - Spectrum use and allocation might change rapidly
  - New waveforms required to cope with changing environment
  - Collaboration / compatibility with existing and new systems
- EO systems need to be adaptive
  - Improved classification and scouting
- It is expected that even during the mission the need for on-board processing grows and updates become necessary

/// Main Requirements

- Latest edge MPSoC (combination of FPGA and processors)
- Nanosat compatible SWAP: <0.5U, few 100 g (whole stack)
- Better performance-per-watt compared to Z7030
- Power range: 10W – 20W
- Enable use of COTS in processing section, including COTS O/S and S/W, separate space specific functions

Solutions for Advanced Nanosat Payloads

/// "Classical" RadHard Systems

- Use RHBD chipsets
- Less performant, no access to latest chips
- No access to latest toolchains, Higher costs
- Flight proven, Known reliability

/// Dedicated "COTS only" systems

- Use COTS with some characterization
- Typically Hardware mitigations (de-latch) only
- Better confidence than bare COTS
- Simple, proven design
- Flight proven, known reliability (but less than RHBD)
- Longer time to flight, since characterization takes time, otherwise higher risks, Still part selection is limited

/// Hybrid systems – best of two worlds

- Mixture between COTS and radhard supervisor
- Differ in the way how to implement the supervisor
  - Simple FPGA: basic, robust supervision
  - *Complex µP: advanced, adaptive, dynamic supervision*
- Can take more risks in the COTS part of the payload

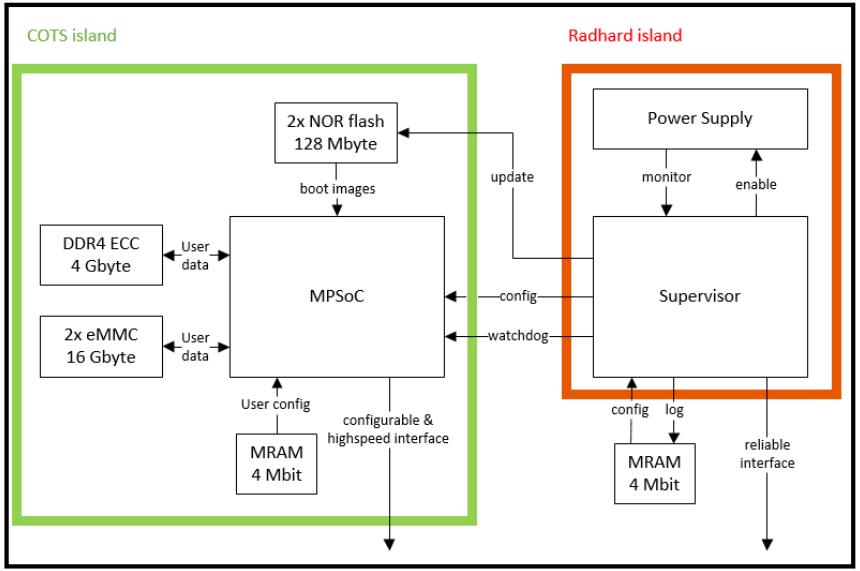
S/W and F/W considerations

- Direct re-use of COTS routines, blocks, libraries possible?
  - *Use standard COTS – e.g. standard Linux: may experience some issues, mitigations required*
  - *Use slightly enhanced COTS – use "low hanging fruits" for in-place mitigation, but still rely on external mitigations*
  - Use hardened S/W and methods, e.g. lockstep, voting: requires considerable effort; more and more difficult to use standard COTS libraries
  - Use bare metal with ultimate low-level mitigation: best possible mitigation, but highest effort.
- **At TAS, we target the first two use cases**

Answer to this need: multiMIND core

TAS multiMIND – core Architecture

multiMIND processing system



/// Basic principle: separation into two main domains

Clever separation into domains, maximizing benefits of two worlds

/// RadHard Island

Goal: Latch-up immune, “always” available (very high availability)

- RadHard power supply (including main parts of COTS domain)
- RadHard ARM M4 SoC (with peripherals: ADC, DAC, COM)
- Power supply monitoring – latch-up mitigation (including extensions)
- Watchdog for COTS FPGA and COTS processor (including extensions)
- Independent upload of critical MPSoC software elements
- Gathering of crucial HK status
- Critical / reliable TM/TC endpoint

/// COTS Island

Goal: Survives in space, controlled by RadHard supervisor

- Provides calculation power, FPGA space and specialized ressources (AI accelerator)
- Xilinx Ultrascale+ MPSoC plus specific frontend, mission and accelerator add-ons
- Manages mission data storage
- Handles mission interface boards (digitizer / RF frontends)

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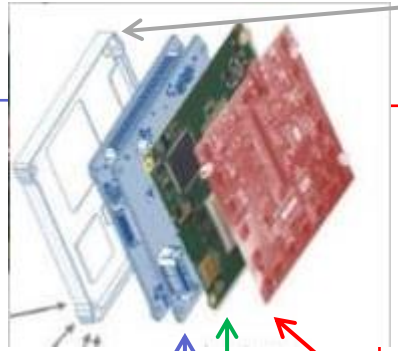
TAS multiMIND - stackup



/// Heat Spreader

/// Mission Board (required)

Interface to OBC and to real world (digitizer)

Interfaces to platform:
- Combines Xilinx and Vorago interfaces
- Level shift (CAN, UART, Ethernet PHY)
- Interface to satellite power
  - 5V or 12V regulated or NRB battery
  - Supplies additional boards (FMC or companion board) including monitoring line to supervisor

Digitizing Frontend:
- High speed I/F (JESD204B, total > 100 Gbit/s) to digitizers (ADC, DAC), multi channel and/or wide band
- High speed I/F to transceiver chips (AD series)

/// Companion Boards (optional)

- Highly mission specific add-on boards
- Using always generic multiMIND core

Examples:
- AI accelerator (Intel Myriad X VPU)
- Phyased Array radar preprocessor (RFSoC)
- High Performance GPU or ASIC

Features:
- Main power rail monitored / enabled by supervisor
- Simple interfaces to multiMIND (SerDes, USB3, …)
- Companion is not mission critical; payload can operate in degraded mode without companion
- Companion can be designed simple; lowers NRC, accelerates time to orbit

/// Core Board

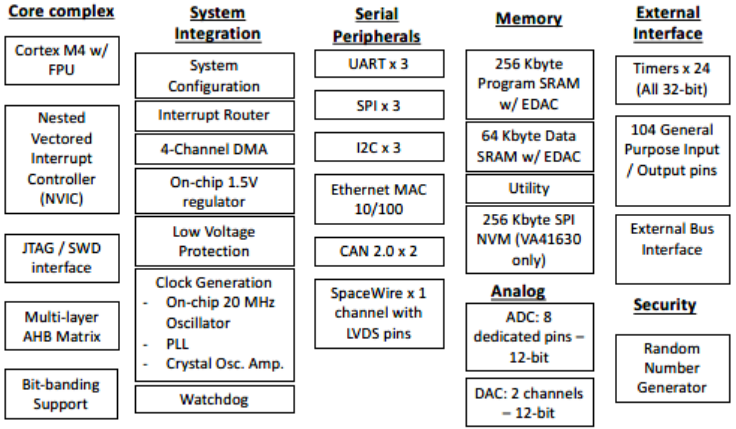
MultiMIND core payload processor (details see later) – main topic here …
- Generic core, present in any payload

Symbolic picture, does not depict thermal design

Hardware (Supervisor SoC)

/// Radhard Supervisor processor

- Vorago VA41630 (ARM M4), “all-in-one”
  - 100 MHz clock, FPU
- Powerful SoC with integrated memories, interfaces and peripherals
  - FRAM program storage memory
  - EDAC program execution and data (SRAM) memory with scrubbing
  - Hardblock communication interfaces (UART, SPI, CAN, Ethernet, [SpW])
  - 12bit ADC / 12 bit DAC on chip
  - Lots of GPIO, timers, …
- Radiation hardened (Vorago’s proprietary hardsil process)
  - SEL immune
  - Low SEU; most memory EDAC protected
  - TiD robust (> 200 krad as PEM)



Source: Voragotech

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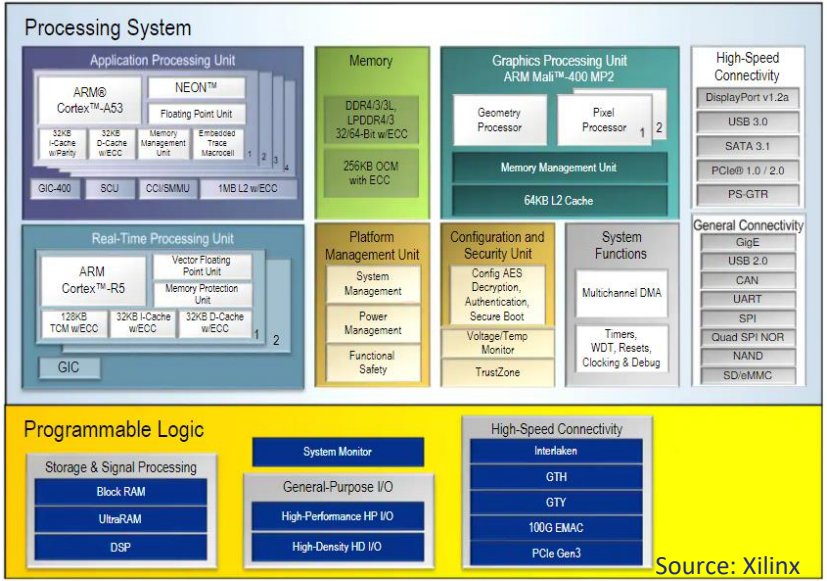
Hardware (payload processor MPSoC)

/// Xilinx Zynq Ultrascale+ MPSoC

- Quadcore ARM A53 with Neon FPU; Mali 400 GPU
- Dualcore A5 RPU
- High speed I/F available to OBC (including Gigabit Ethernet)
- Large FPGA (multiMIND features ZU6EG, ZU9EG and ZU15EG; same footprint - selectable according to FPGA size needs)
  Smaller FPGA → lower power; large FPGA → max performance
  - Up to 341k CLB-LUT, 3528 DSP, 26 Mb BRAM, 31 Mb URAM
  - 12 GTH (12.5 Gbit/s) available to FMC

Radiation behavior:

- Power Supply uses radhard components (mainly SEP PoL), capable of 18 Amps on core rail
- Improvements against Zynq Z7xxx series (ECC caches, improved processor section)
- But unfortunately: some SEL issues requiring attention
- **Not** using MIL grade Ultrascale+ in undervolt mode (need the IO banks), but monitoring the rails by supervisor



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Hardware – memories

multiMIND memories	
Working memory	4 Gbyte DDR4
NV code memory	2x 128 Mbyte NOR flash
NV data memory	2x 16 Gbyte eMMC (pSLC)
NV config memory	2x 4 Mbit MRAM

/// M4 NV memories

- FRAM code storage (integrated in chip) – 256 kByte
- MRAM config and data storage (external chip) – 512 kByte

/// Shared memories

- 2 * NOR flash – 128 Mbyte, multi-master SPI for M4 and Ultrascale+
  - R/W access from Vorago and Xilinx side
  - Boot loader for A53 subsystem
  - O/S storage for A53 subsystem
  - FPGA bitstream

/// MPSoC NV memories

- MRAM config and data storage – 512 kByte
- 2 * NAND eMMC flash – 16 Gbyte in pSLC mode

Case	Mirror 1	Mirror 2	Equal	Action
1	valid	valid	true	Take Mirror 1
2	valid	invalid	false	Repair M2, Take M1
3	invalid	valid	false	Repair M1, Take M2
4	valid	valid	false	Repair M2, Take M1
5	invalid	invalid	true	Use Factory Settings
6	invalid	invalid	false	

Truth-table for using memory images

/// Error protection

- MRAM and FRAM cells are SEU immune (but R/W can suffer from SEU); block copies and CRC
- NOR data is CRC protected (within files); multiple images; two chips for redundancy
- NAND data is ECC protected (internally); two chips for redundancy

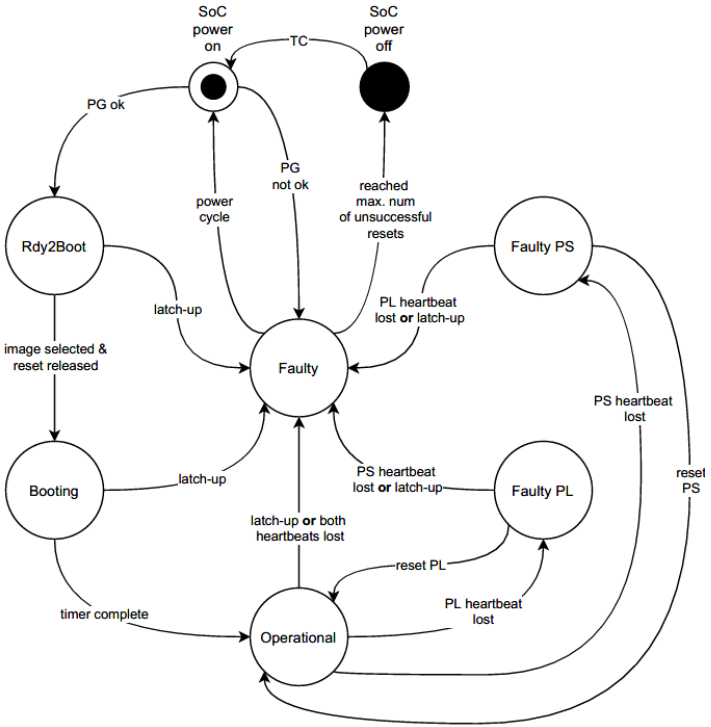
Operation – boot-up logic / update

/// Boot-up

- Vorago supervisor boots up from internal code (FRAM)
- Vorago selects NOR flash, which is used to boot the Xilinx
- Vorago controls the entire boot process and reports HK status to OBC
- Vorago controls “return to Golden Image” or “return to last image”
- Xilinx fetches FSBL, SSBL, O/S and FPGA bitstream from NOR flash. Multiple copies of each are available in each NOR flash

/// Update (during flight)

- Vorago: Self-update possible (currently not implemented)
- Xilinx:
  - Boot device (NOR flash) accessible by Vorago and Xilinx
  - S/W update possible by both devices
  - S/W update possible when some MPSoC S/W is broken and Xilinx does not boot
  - Data scrubbing to prevent accumulation of errore
  - “previous image” and “Golden image” is always kept in case update fails.



Simplified state machine controlling MPSoC boot and monitoring

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Radiation Effects Mitigation

/// Supervisor

Supervisor shall protect the COTS island from destructive effects and shall provide mitigation against SEU/SEFI etc.

- Supervisor O/S foresees some mitigations in H/W and S/W
- Hardware mitigations
  - Radhard island (see above), radhard power
  - Redunant storage chips
  - Multiple images stored with CRC (integrity check)
- Software mitigations
  - Data scrubbing
  - Watchdogs
  - Sanity checks
- Combined
  - Latch-up detection and control

/// Ultrascale+ MPSoC

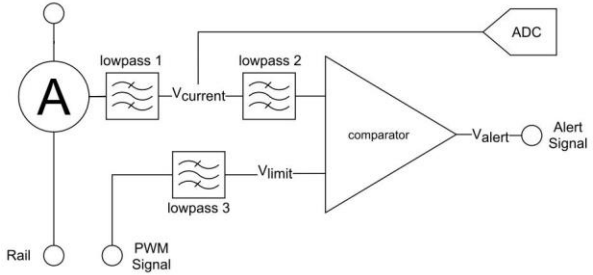
- This chips holds the mission specific code, so radiation mitigation responsibility is up to the user.
  However: the supervisor protects this section; survival and basic availability is ensured.

- Some library elements, especially COTS O/S [Linux] have little radiation mitigation. They implicitly rely on the watchdog.
- Use functions, where available (e.g. ECC, data scrubbing, watchdogs)
- As a general rule, S/W shall be implemented in a robust and defensive way:
  - Implement sanity checks, range checks
  - Be prepared of bit / byte errors in input and output, act defensively
  - Do periodic checks (scrubbing, read-after-write)
  - Secure critical operations by multiple trigger points
  - Be prepared of resets / reboots and manage graceful continuation of interrupted operations

Latch-Up Mitigation (Overview)

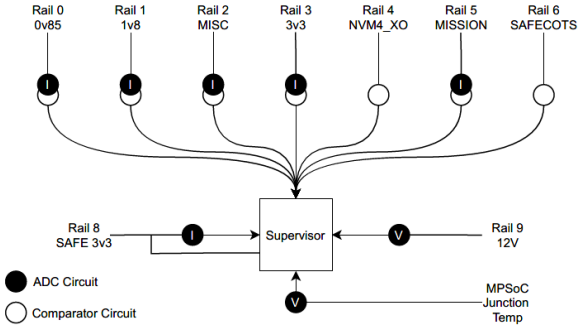
/// RadHard power supply stage with current monitoring

- (active) EEE parts in power supply stage are radhard
  - Latch-up immune up to >43 MeV cm²/mg [@ 125°C, but usually operated much lower]
  - TiD assured to 20 krad, characterized to 30 krad
  - SET characterized for critical components
- Using SEP (plastic encapsulated) where available



/// Two stage protection

- Current monitoring with space grade (SEP) amplifiers, comparators and µC
- **Fast CutOff:** Comparator generates alert signal, when current exceeds adjustable (PWM) threshold.
  Signal generates an interrupt which disables the PoL.
- **Adaptive Slow CutOff:** Current is analyzed; if measured current shows suspicious signature, PoL is disabled.



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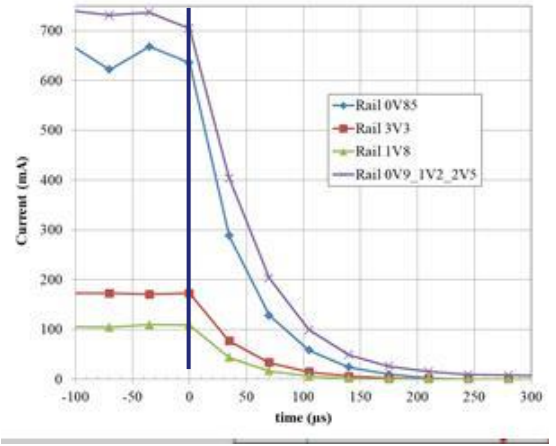
Latch-Up Mitigation (Performance)

/// Power down by pulling enable signal of PoL

- Advantage: No additional radhard component required (floor space, component costs)
  No additional component within the high power section of the rail
  (important for high current rails)

/// On-board current measurements and threshold control

- Current on main rails is monitored by integrated ADC in M4.
- Monitoring all channels yields to some 10 kHz (100 µs) sampling interval → used for nominal ops.
  Monitoring a single channel yields to 200 kHz.
- Data is buffered in ring buffer available for „post-latch-up“ dump
  Allows measurement and characterization of „real“ latch-up events during the mission
- Fully configurable:
  - Fast CutOff thresholds can be S/W changed respecting the current operation state, including start-up or init.
    Can consider state-dependant changes in rail currents (e.g. GTH on/off).
  - Slow CutOff is detection algorithm fully under S/W control; „alert-law“ is configurable; can also use current slopes or combination of measurements.



Self-monitored MPSoC power down
(data available via TM link afterwards
„test-while-you-fly“)

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Software Aspects

/// Separate Supervisor and COTS Islands

Goal: Reduce development time of mission specific FPGA and S/W
Use known COTS libraries for space (e.g. SIGINT, vision, AI, …)

/// Supervisor Island (M4 supervisor)

- Supervisor O/S provided by TAS (generic, but extensible)
- Ensures critical functions
- TC endpoint, continuous HK delivery
- Customer can include own elements / tasks / add-on

/// COTS Island (Ultrascale+)

COTS applies also for FPGA and S/W.

- BSP provided by TAS (derived from Xilinx Vivado/Vitis)
- O/S selection and software is mission specific and customer responsibility (TAS can provide support)
- FPGA development is mission specific and customer responsibility
- Due to standard interfaces (FMC, Ethernet, SerDes), standard blocks can be integrated

"This the first time we'll be flying Linux on Mars. We're actually running on a Linux operating system. The software framework that we're using is one that we developed at JPL for cubesats and instruments, and we open-sourced it […]. It's kind of an open-source victory […]"

Tim Canham, NASA Mars Helicopter Operations Lead
https://spectrum.ieee.org/automaton/aerospace/robotic-exploration/nasa-designed-perseverance-helicopter-rover-fly-autonomously-mars. (17.02.2021 - fetched 17.05.2021)
Image taken from NASA website.

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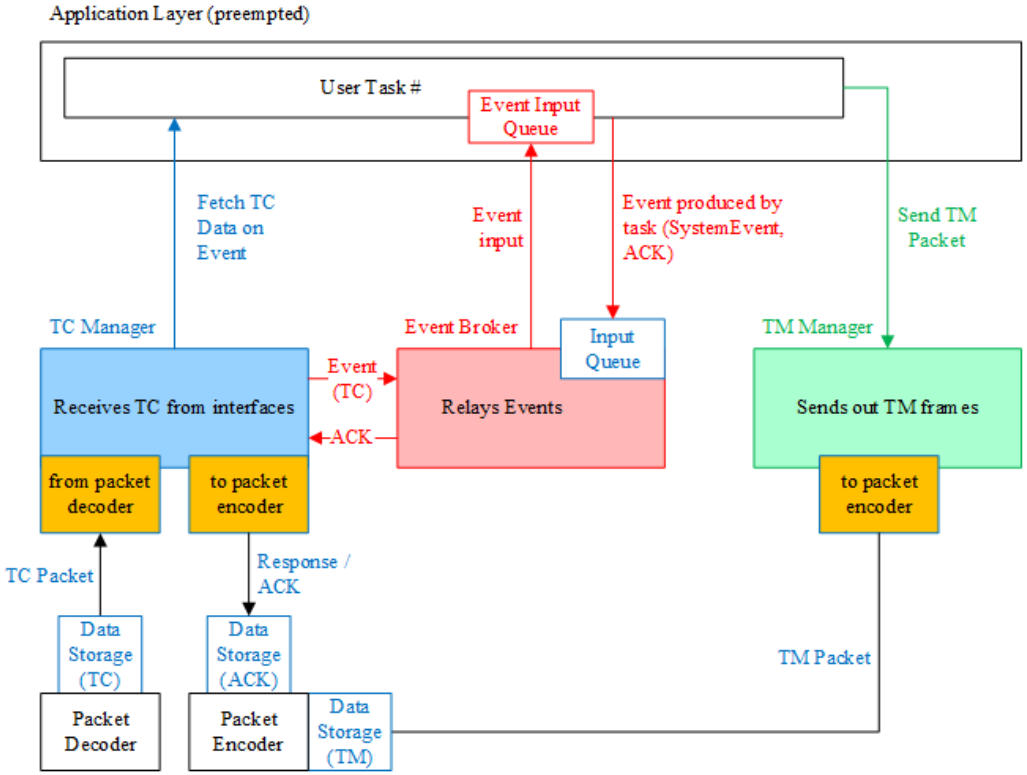
Software aspects – Supervisor Island

/// Supervisor O/S

- Generic O/S for multiMIND family
- Based on FreeRTOS kernel
- Generic, customizable TC/TM/HK handler
- Layered extensible structure

Main features

- Scalable for different protocols
- **Fully configurable** TM/HK generation and rates, including in-flight reconfiguration
- Generic handling regardless of interfaces
- **Accepts specific user tasks**
- Provides TC/HK/Event infrastructure also to user tasks in the same way as for system tasks



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Software aspects – COTS Island

/// Ultrascale+ A53 quad core processor

- Foreseen to run COTS OS (e.g. Linux – but in principle fully open) with standard drivers
  - Ready-to-use CCSDS, PUS, CSP … handlers
  - Journalling file systems
  - IIO driver to various hardware (AD9361 and beyond …)
- No specific space S/W blocks / elements required (but could be added …).
- A53 has already some basic hardening: ECC caches (partly L1, full L2), ECC DDR memory

/// Ultrascale+ R5 dual core processor

- Possible lockstep operation. FreeRTOS available.
- Intended for “semi-critical” domain (e.g. extended FPGA scrubbing, critical watchdog, state-machine-monitoring)
- Will “survive” Linux / FPGA reboot, but will be affected on MPSoC power-down
- Currently not used; TAS can provide specific applications.

/// Ultrascale+ FPGA

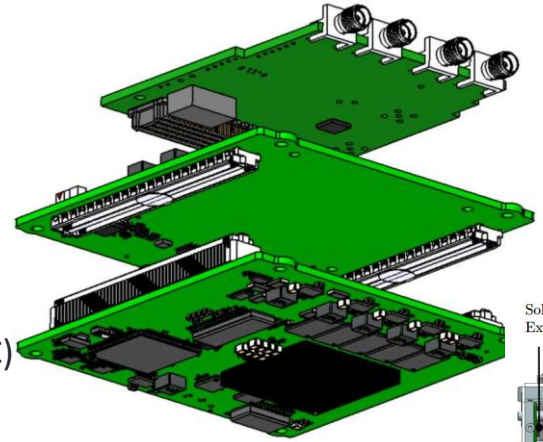
- Under customer control (except some H/W accesses, which are provided as BSP)
- Some simple mitigations possible: CRAM scrub, ECC on memories etc.
- Further mitigations up to the user (TMR)

Current Missions

/// EIVE (flight scheduled 2022)

Boards:

- MultiMIND core
- Mission board (with FMC I/F)
- COTS FMC board (high speed DAC)
- Heat Spreader

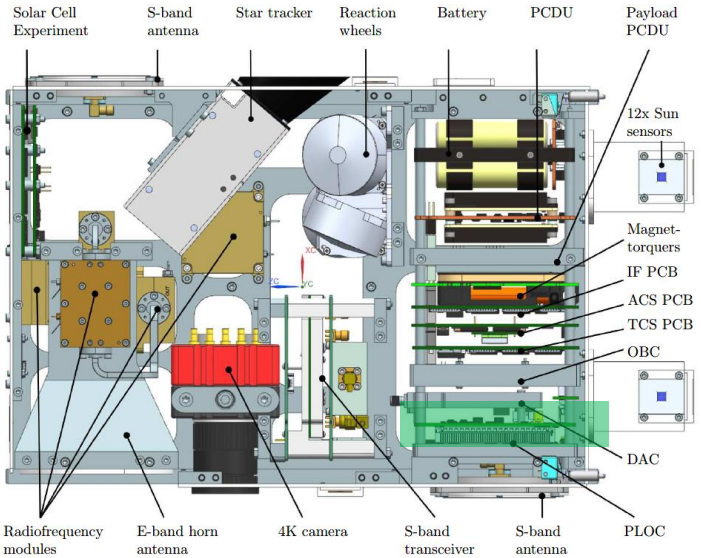


multiMIND PCB stack for EIVE (exploded view):
Top: COTS FMC board („frontend“)
Mid: mission board, holding FMC I/F and satbus I/F
Bot: multiMIND code board; heat dump to the bottom

/// ESA AIoT (AI testbed, EM 2022/2023)

Boards:

- MultiMIND core
- Mission board (with FMC I/F)
- COTS FMC RF transceiver (AD9361)
- AI accelerator companion (Myriad X)
- Heat Spreader



EIVE 6U cubesat (credit: IRS Uni Stuttgart); multiMIND PCB stack in **green rectangle**, labelled as DAC [mission board] and PLOC

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Summary & Outlook

/// Hardware

- MultiMIND as enabler for high performance payload processing
- Hybrid single board solution combining radhard and COTS
- **Open commercial product (“web shop”) or part of a payload solution**

/// Software

- Generic, **open supervisor O/S [included with H/W]**
  - Collaborative developed open & routines (e.g. protocol handler)
  - **Intended for wide distribution (collaborative license model) [included w. H/W]**
- Development starts with COTS hardware – before flight boards are available
  - COTS section compatible with standard breadboards (Trenz Electronics), EBB / flatsat is available as COTS version
  - Simplify and accelerate development; shorten time to flight; include characterization

/// Applications (payloads)

- Flexible to cover various applications, especially
  - RF signal processing (complex waveforms, smart antenna, wide band spectrum)
  - Signal intelligence, AI assisted video processing
  - Characterization missions for new, powerful chipsets and hardware

multiMIND commercial product

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Thank you for yor attention

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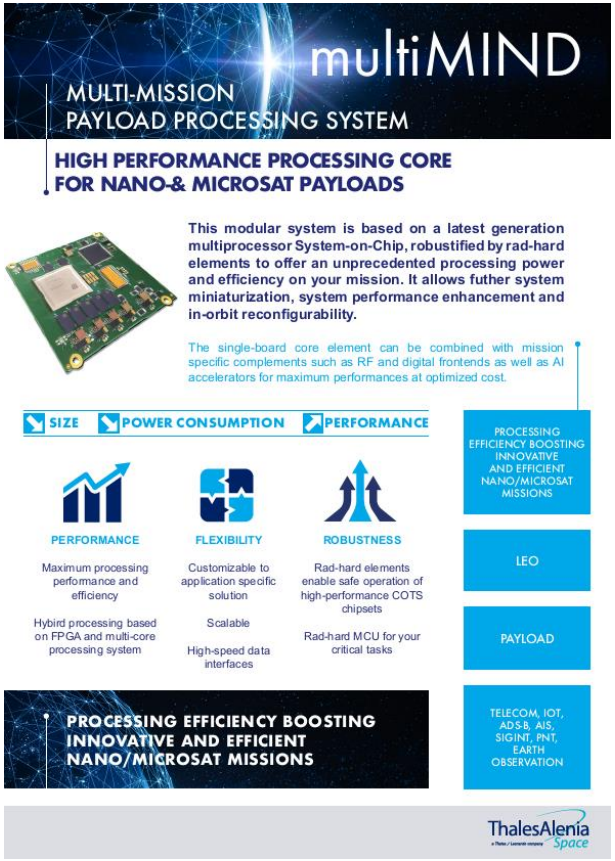

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