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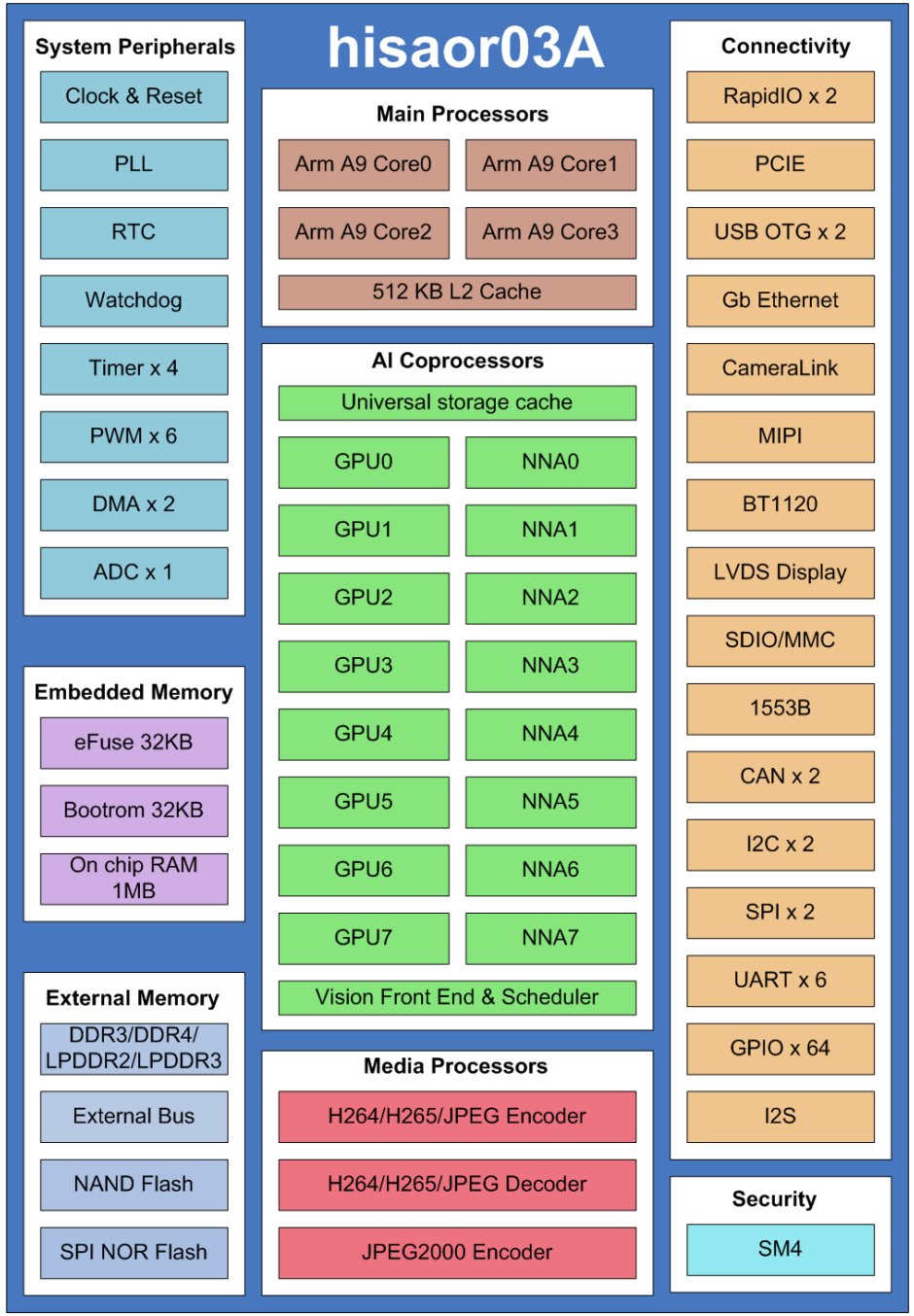
The **hisaor** chip - a new system-on-chip that combines advanced neural network and digital signal processing with multiple interfaces, radiation tolerance, and low power consumption.

Barry Kavanagh, Michael Ryan



Main processor	4 core ARM A9
AI coprocessor	GPU*8+NN*8
Production process	FD-SOI 22nm
Floating point computing power	64GFLOPS
Fixed point computing power	12 TOPS
Main frequency	1GHZ
Temperature class	【-40 , 125℃】
Typical power consumption	6W
DDR type	64bit DDR3/DDR4
Video codec	H264/H265/JPEG2000
Encryption and decryption engine	SM4
Package size	25*25mm

Evaluation board & demo setup

Neural network image processing demo

- The neural network approach involves two main stages
- Training
  - Decide on a neural network configuration and set the weights so as to minimise total error across a large number of pre-classified images
  - Result is a NN model expressed in a standard way.
  - (Have done this with *hisaor*, but usually done off-line in cloud etc.)
- Using
  - Set up system to run the model
  - Feed in an object to be classified
  - Look at the classification probabilities

Yolo Model and Satellite Image

Yolo both detects and classifies.

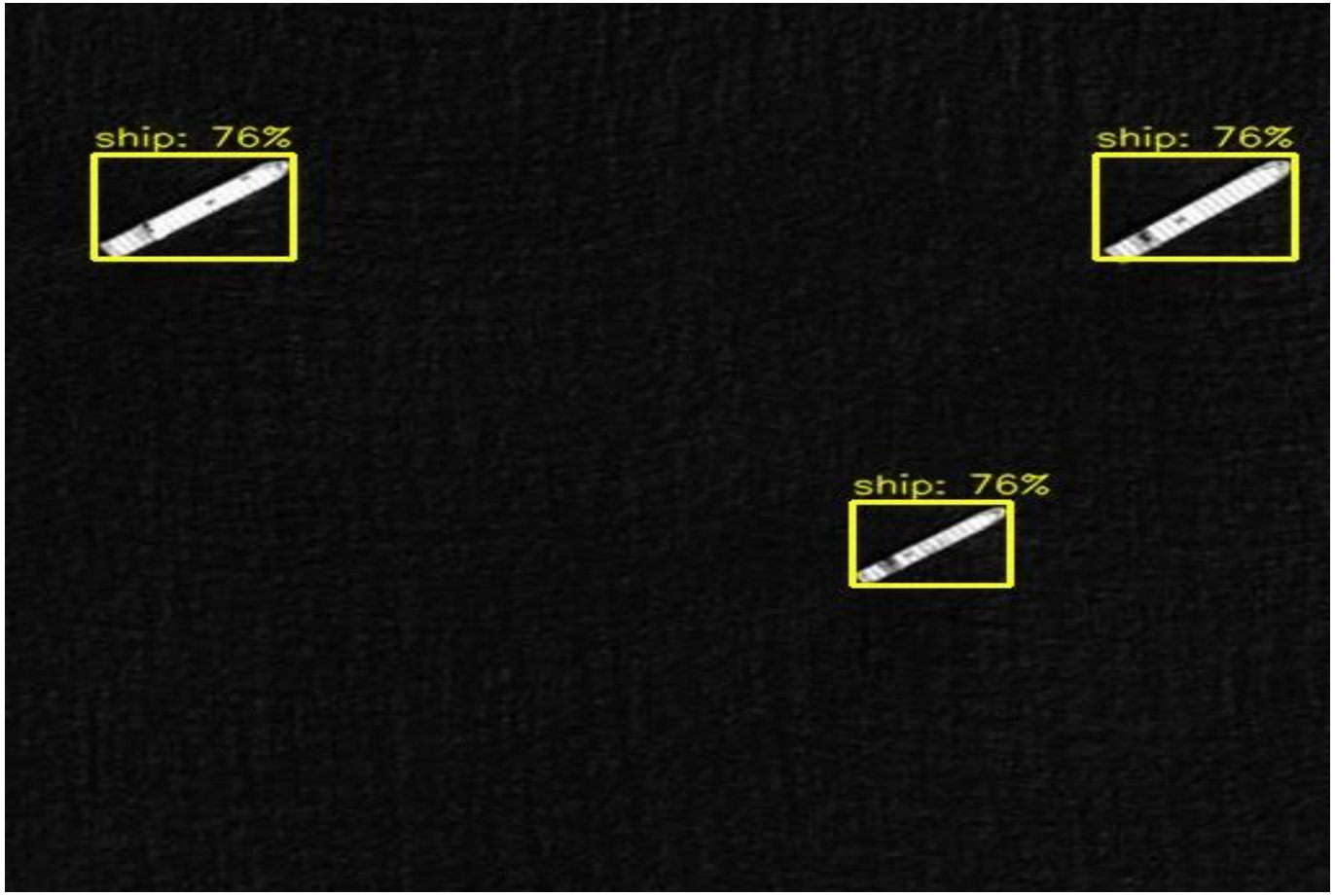
Any things there?

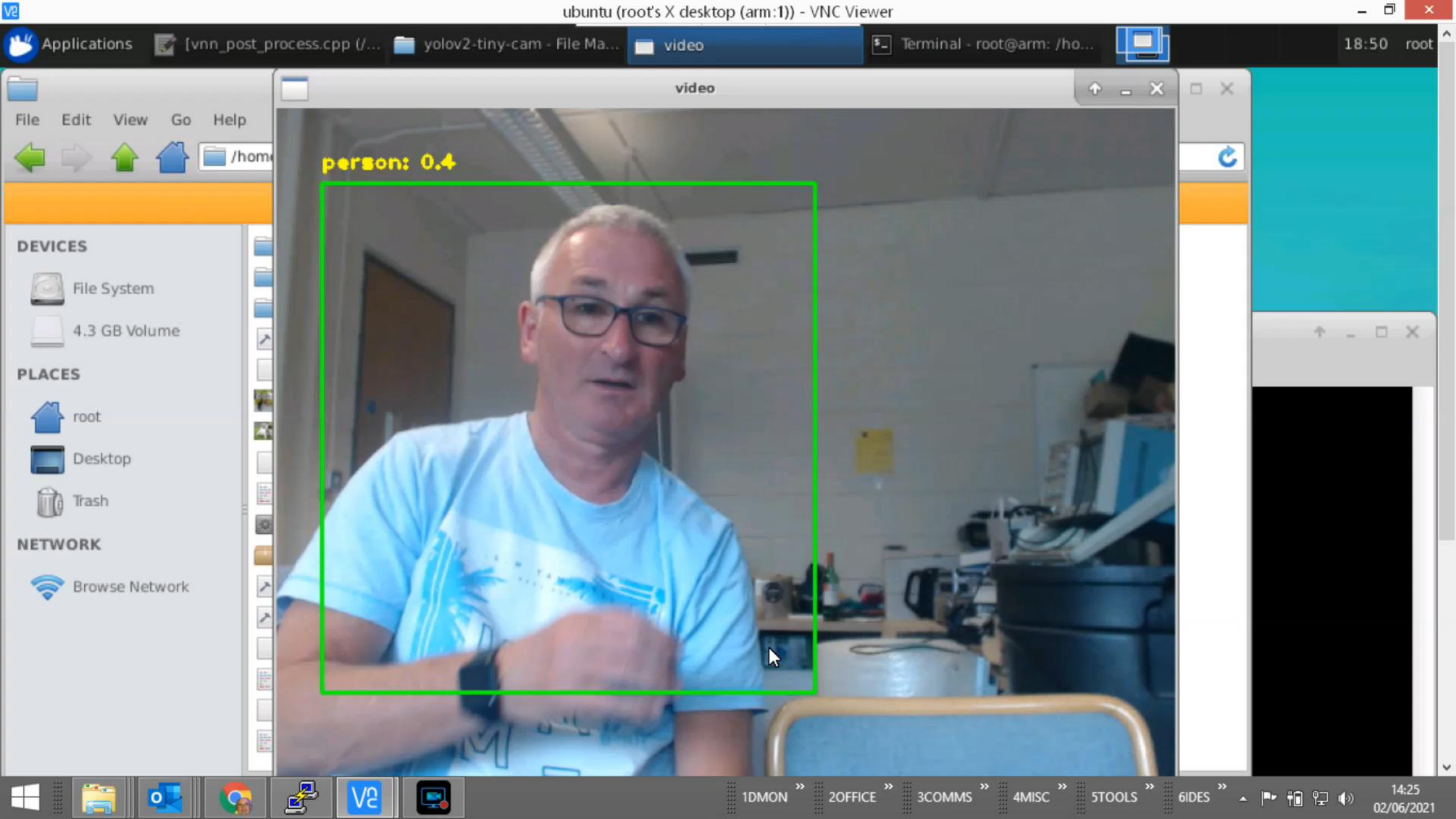
Where are they?

What are they?

(Ans.:Three ships)

hisaor time < 5 ms




ubuntu (root's X desktop (arm:1)) - VNC Viewer
Applications
[vnn_post_process.cpp (/...
yolov2-tiny-cam - File Ma...
video
Terminal - root@arm: /ho...
18:50
root
File Edit View Go Help
DEVICES
File System
4.3 GB Volume
PLACES
root
Desktop
Trash
NETWORK
Browse Network
video
person: 0.4
1DMON
2OFFICE
3COMMS
4MISC
5TOOLS
6IDES
14:25
02/06/2021

How the demonstrations were made

- On PC:
  - Use Acuity IDE to create version of Yolo for use on hisaor
    - Uses OpenVX
- Evaluation board
  - Connect terminal and camera to evaluation board
  - Power up evaluation board
  - Use terminal to identify OS location (SD card with Linux Ubuntu)
  - Log in to Linux over Internet
  - Download and start application
- Things worked as expected!!!

Back to the chip

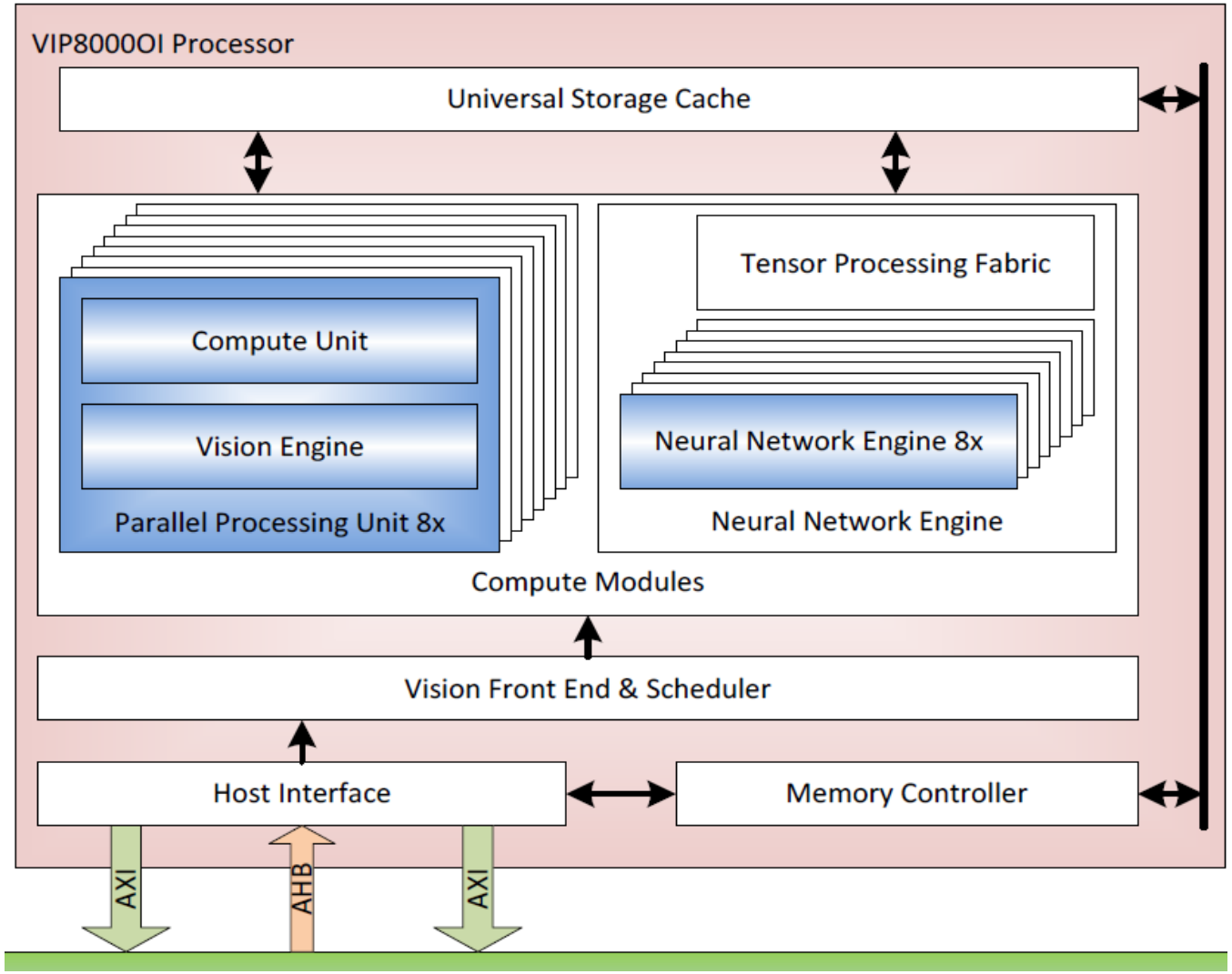
- All our own work? NO!!
- Many IP cores from different vendors
  - Some with space heritage already
  - All from established vendors
  - All with appropriate support software
- Designing
  - What criteria must the IP cores meet?
  - What functionality would be good to have?
  - What corresponding cores meet the criteria?
  - How best to connect them?
  - On-chip vs off-chip memory

Some Design requirements

- Low power consumption and good radiation tolerance
- Fast image processing
  - Capturing the image
  - Processing the image
- Fast NN processing
  - Numerical throughput
  - Software compatibility
- General purpose processing
  - Good processing power
  - Able to run Linux
- Interfaces – as many types as possible

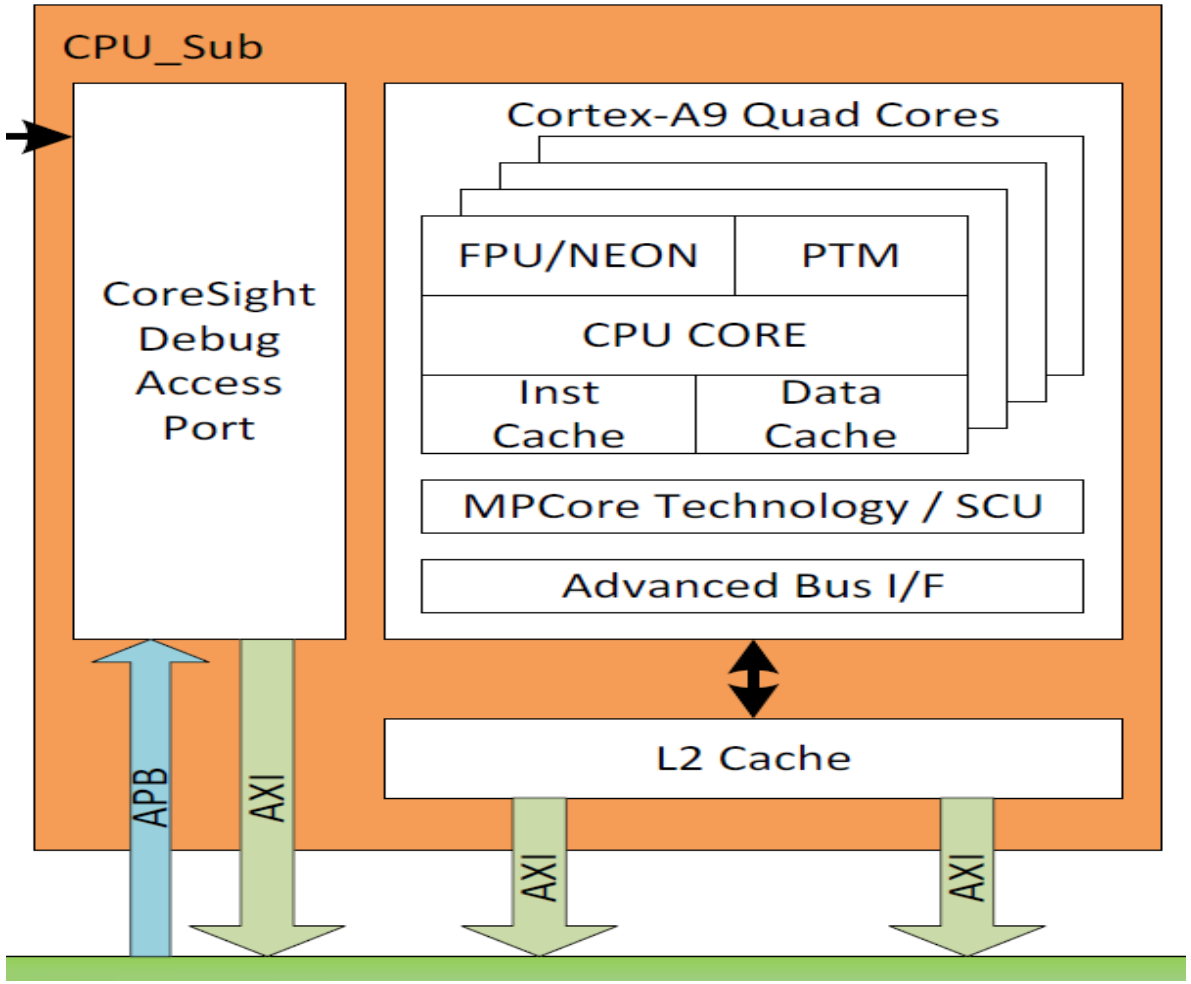
NN processing system

- 8 x GPUs
- 8 x NN processors
- Shared high speed cache
- High speed connectivity
- At max 1 GHz clock
  - 64 GFlops
  - 12 TOPS



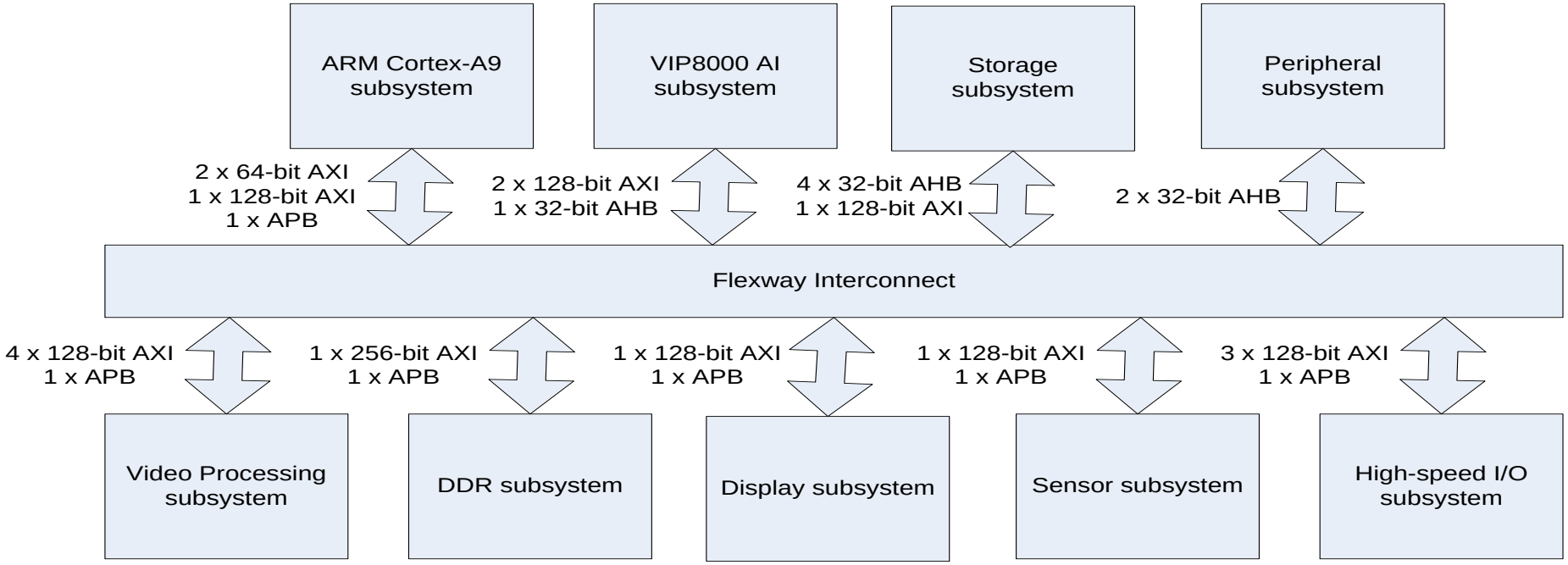
Central CPUs

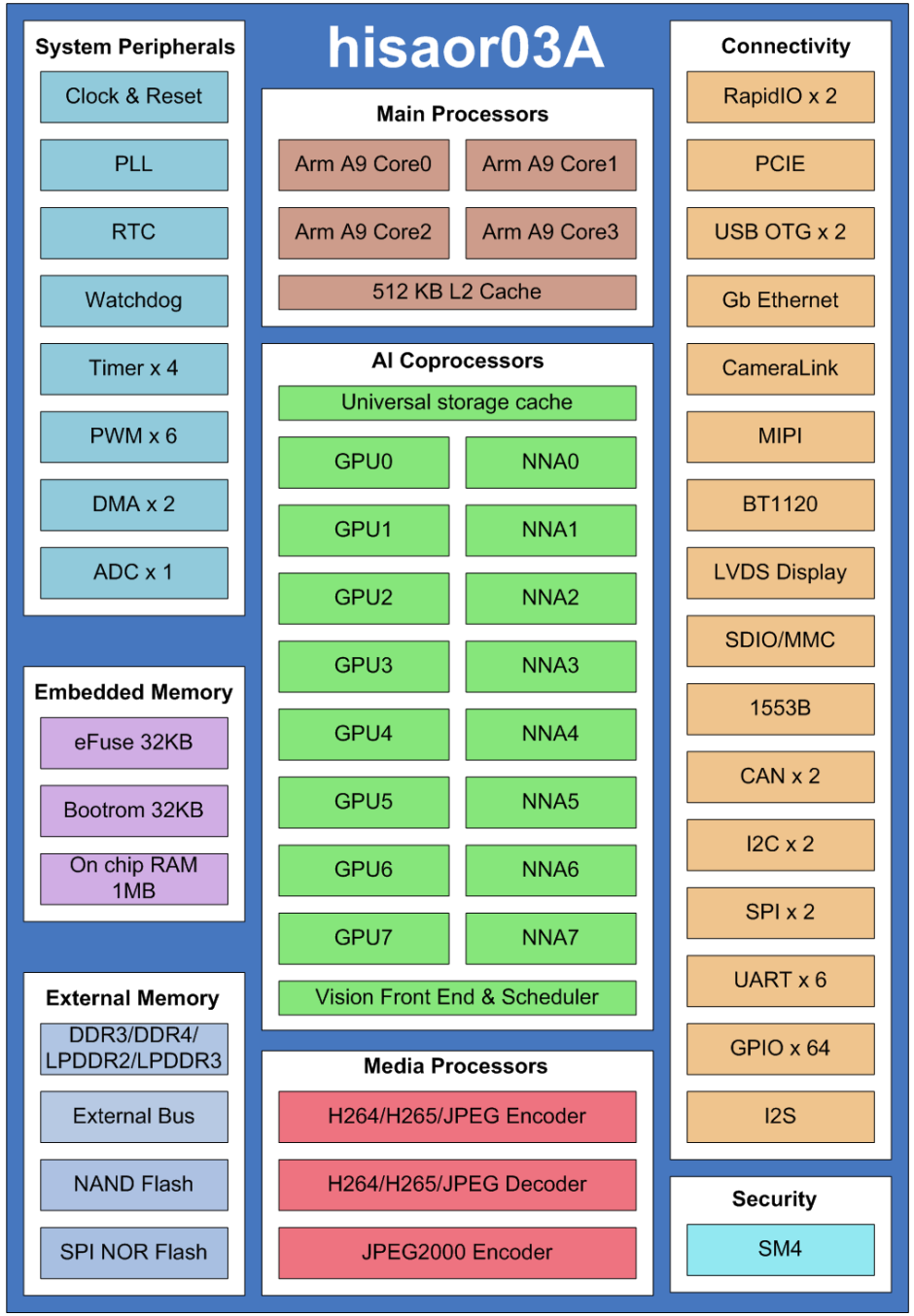
- 4 x ARM Cortex-A9
- With FPU & SIMD
- 32 KiB Level 1 caches
- 512 KiB Level 2 cache
- High speed connectivity
- Coresight Debug access



Only connect…

With many IP cores and a need for the highest possible bandwidth the on-chip bus design was far from simple:





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Acknowledgements

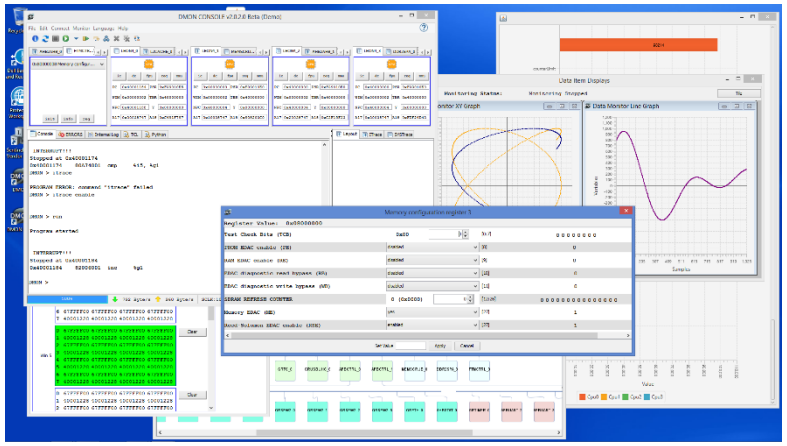
The *hisaor* chip was made possible by a lot of people in a lot of organisations.

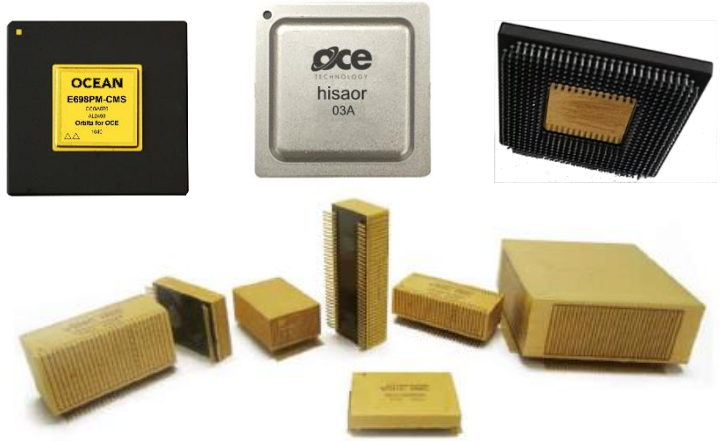
While it is impossible to mention them all, we must in particular thank

Zhuhai Orbita Aerospace Science & Technology Co. Ltd. whose staff made a major contribution to both the design and implementation of *hisaor.*

Our thanks are also due to VeriSilicon Microelectronics Co., Ltd., who provided some of the main IP cores used in *hisaor* and were helpful throughout the project, and to the KHRONOS group for their work in relation to AI software.

Questions?





Embedded software tools, Hi-rel components, & Satellite Subsystems