

ASTERIA: New Development of a Highly Miniaturized Space Monitoring Camera

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ABSTRACT

Reducing the size, mass, cost, and delivery time of space payloads has become a key priority for the space industry. This trend also applies to onboard cameras, whose use is rapidly increasing as essential tools for payload and mission monitoring. However, these improvements must not compromise performance, quality, or reliability, which remain critical to mission success. Meeting these objectives therefore requires significant architectural and design trade-offs. This paper presents 3D PLUS development of the ASTERIA space camera, addressing these challenges through a highly integrated optoelectronic architecture and mechatronic design.

The paper discusses the application context and main system requirements, the architectural and component selection trade-offs, and the development of the ASTERIA optoelectronic core. The integration of the core with the optical and mechanical subsystems is then presented, together with preliminary results obtained during the ongoing development. The current development status and remaining activities toward the final camera configuration and qualification are finally discussed.

Keywords: Space, Camera, Optoelectronic Core, Miniaturization, Monitoring, CMOS image Sensor

1. INTRODUCTION

Context and Motivations

The increasing use of imaging systems in space missions is driving a growing demand for compact, low-power, and cost-effective space cameras. Beyond traditional payload and platform monitoring applications, cameras are increasingly considered as enabling instruments for proximity operations, navigation, inspection, and situational awareness. This trend is expected to accelerate with the development of high-volume satellite constellations, private space missions, and the increasing number of exploration missions targeting Earth orbit, the Moon, and deep-space environments. In particular, the renewed interest in lunar exploration and the broad range of missions considered within the Artemis program are creating new opportunities for compact, ready-to-use, and affordable, imaging systems operating in increasingly constrained environments.

At the same time, space cameras remain subject to stringent system-level constraints. Mass, volume, and power consumption must be minimized while maintaining the image quality, reliability, and environmental robustness required for space applications. Cameras must withstand radiation, thermal variations, mechanical loads, and long operational lifetimes, while providing high-quality images with potentially high framerate to accommodate more demanding applications. The adoption of high-speed digital interfaces, such as Ethernet, together with increased onboard processing capabilities, provides new opportunities to improve camera architecture and simplify interfacing to the most recent commercial space platforms, but also introduces additional challenges in terms of power consumption, thermal management, signal integrity, and system complexity.

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Conventional space camera architectures, while providing flexibility and benefitting from mature technologies, often result in significant volume, mass, power consumption, and development costs, while potentially limiting the achievable level of processing capability and physical integration.

These competing requirements highlight the need for new camera architectures combining high integration, space compatibility, processing capability, while targeting cost optimization and volume manufacturing to address the developing market. This approach is the basis of the ASTERIA camera development.

ASTERIA Concept

Building on the heritage of 3D PLUS CASPEX Camera Heads [1][2] and the associated IRIS Cameras, ASTERIA (As depicted in Fig. 1) is developed as a compact space camera architecture addressing the increasing demand for low SWaP-C imaging systems without compromising the radiation hardness, reliability and environmental performance required for space applications. The camera is designed to provide a turn-key imaging solution combining the optical assembly, image sensor, processing electronics, and camera interfaces within a highly integrated and compact architecture.



Figure 1. Rendering of ASTERIA Wide Angle Space Camera (P/N: 3DCS08M051011-1 – Ethernet configuration).

The targeted applications cover a broad range of space missions, including payload and platform monitoring, inspection, situational awareness, and imaging functions for Earth-orbiting, lunar, and deep-space missions. The architecture is also intended to address applications requiring multiple cameras or distributed imaging systems, where camera size, power consumption, and integration effort can become significant system-level constraints.

The main design objectives of ASTERIA are therefore to achieve a significant reduction in size, mass, and power consumption while providing high-quality imaging, high-speed data transmission, and sufficient onboard processing capability. The architecture has also been designed with space-specific requirements in mind, including component reliability, thermal management, radiation considerations, and long-term product availability.

One of ASTERIA architecture main feature is the integration of the main optoelectronic and processing functions into a dedicated optoelectronic core, based on 3D PLUS patented 3D Stacking technology, benefitting from more than 30 years of space heritage, and used with success for its CASPEX Camera Heads product line. This high level of integration allows for enhanced miniaturization level of the optoelectronics core of the camera while contributing to a more tightly integrated mechatronic and optical design.

System Requirements

The ASTERIA camera architecture is defined from a set of system-level requirements driven by the targeted monitoring and inspections applications, in addition to the goal to optimize the size, mass, power consumption and cost.

The main inputs considered during the preliminary architecture definition are summarized in Table 1.

Table 1. ASTERIA input target requirements

Parameter	Target Value
Image Resolution	8Mpx providing native 4K resolution

Field of View	Wide field of view ($> 80^\circ$ Horizontal) targeting monitoring applications
Spectral Range	Visible, color sensor
Frame Rate	Up to 30 frames per second in 4K resolution, supporting low frame rate imaging
Embedded image processing	Low level image processing: Auto-exposure, white/color/gamma correction, pixel correction, Compression
Communication interface	Gigabit Ethernet, SpaceWire
Input power	5V baseline, Extended 12V targeted
Power Consumption	$< 5W$
Mass	$< 100g$
Volume	Target envelope of $30 \times 30 \times 50 \text{ mm}^3$ (out of mounting ears and potential baffle)
Operating Environment	From LEO to GEO mission, Lunar surface, deep space missions

The resolution and frame-rate requirements aim to support both high-resolution monitoring and lower-resolution, higher-frame-rate imaging modes. The architecture is therefore required to handle the full data throughput associated with 4K color imaging while retaining sufficient flexibility to operate at lower resolutions and frame rates. This dual requirement is particularly relevant for inspection applications, where continuous high-frame-rate acquisition may not be necessary.

The power, mass, and volume targets were identified as key architectural drivers. With a target volume of approximately 45 cm^3 and a mass below 100g g, the camera is intended to provide a compact imaging solution suitable for applications where the available mechanical and electrical resources are strongly constrained.

The communication interface targets both Gigabit Ethernet, providing a high-speed digital link between the camera and recent platforms, and SpaceWire, still widely used in numerous legacy space platforms. The use of a standard high-speed interface also aims to simplify system-level integration while supporting the data rates associated with high-resolution imaging.

The expected operating environment ranges from Low Earth Orbit (LEO) to Geostationary Earth Orbit (GEO), leading to additional constraints on component selection, radiation tolerance, thermal design, and long-term reliability. This extended requirement, however, aims to fill the gap between COTS solution and legacy space design.

2. OPTO-ELECTRONIC CORE

Optoelectronic Core Architecture Overview

The ASTERIA optoelectronic core is designed as a highly integrated digital imaging module combining the image sensor, processing resources, memory, communication interface, and power management functions within a compact architecture.

The imaging front-end is based on an 8 Mpx rolling-shutter CMOS image sensor with a $2\mu\text{m}$ pixel pitch and a 1/1.8 inch optical format compatible with the targeted 4K color imaging capability while allowing the use of compact optical design suitable for the ASTERIA concept. The sensor provides the raw image data in 10 or 12 bits per pixel to the digital processing architecture through a 4-lane MIPI-CSI2 interface, where acquisition, control, and image processing functions are implemented. It also provides basic preprocessing capabilities such as Binning, defective pixels correction, black level correction and HDR in the form of sequential incremental exposure frames for processing. The optoelectronic characteristics of the sensor are given in the table below.

Table 1. ASTERIA optoelectronic core image sensor characteristics

Parameter	Value
Resolution	3840 (horizontal) x 2160 (Vertical)
Frame Rate	Up to 60 frames per second in 4K resolution
Pixel pitch	2 μm
Shutter type	Rolling shutter
Sensitivity	13 ke-/lux.s
Full Well Capacity	7500 e-
Read noise	3.1 e-
Dark current	22 e-/s at 25°C
Dynamic range	74 dB
Package size	8.9 mm x 6.3mm

The main processing resource is based on a Microchip PolarFire SoC MPFS160T, associated with 8 Gb DDR4 memory. The processing core provides both programmable logic resources in its FPGA fabric, and an embedded multi-core RISC-V microprocessor subsystem. This architecture enables the implementation of sensor control, image acquisition, buffering, processing, and communication functions within the optoelectronic core. The DDR4 memory provides the required bandwidth and storage capacity to handle the high data throughput generated by the image sensor.

Two communication configurations have been considered for the optoelectronic core to address different space-system requirements. The first configuration integrates a Gigabit Ethernet physical layer (PHY) together with the associated magnetics, providing a direct high-speed Ethernet interface at the camera level. The second configuration removes the Ethernet PHY and magnetics from the core and provides a SpaceWire interface, offering an alternative architecture for systems where SpaceWire is the preferred onboard communication standard. This common-core approach allows the main imaging and processing architecture to be maintained while adapting the communication interface to the target mission.

The core also integrates the complete power interface required to operate the different electronic functions. The power architecture receives a wide input power supply from 4.5V to 9V (12V possible with restrictions) and generates the dedicated voltage rails required by the image sensor, SoC, DDR4 memory, and communication components with Point-of-Load and internal regulators. Power sequencing, filtering, monitoring, and local regulation are integrated within the core to reduce the number of external interfaces and simplify the overall camera architecture. An Under Voltage Lock Out (UVLO) function is integrated in the design in case of power supply instability, and in the case of SpaceWire configuration, an overvoltage detection is added to the main PoL converters to protect the system and the SpaceWire interface to the platform.

This functional integration results in a self-contained optoelectronic building block combining image acquisition, processing, memory, communication, and power management. The architecture is therefore designed to minimize external components and interconnections while providing sufficient flexibility to support different camera configurations.

The figure hereafter shows an overview of ASTERIA optoelectronic core.

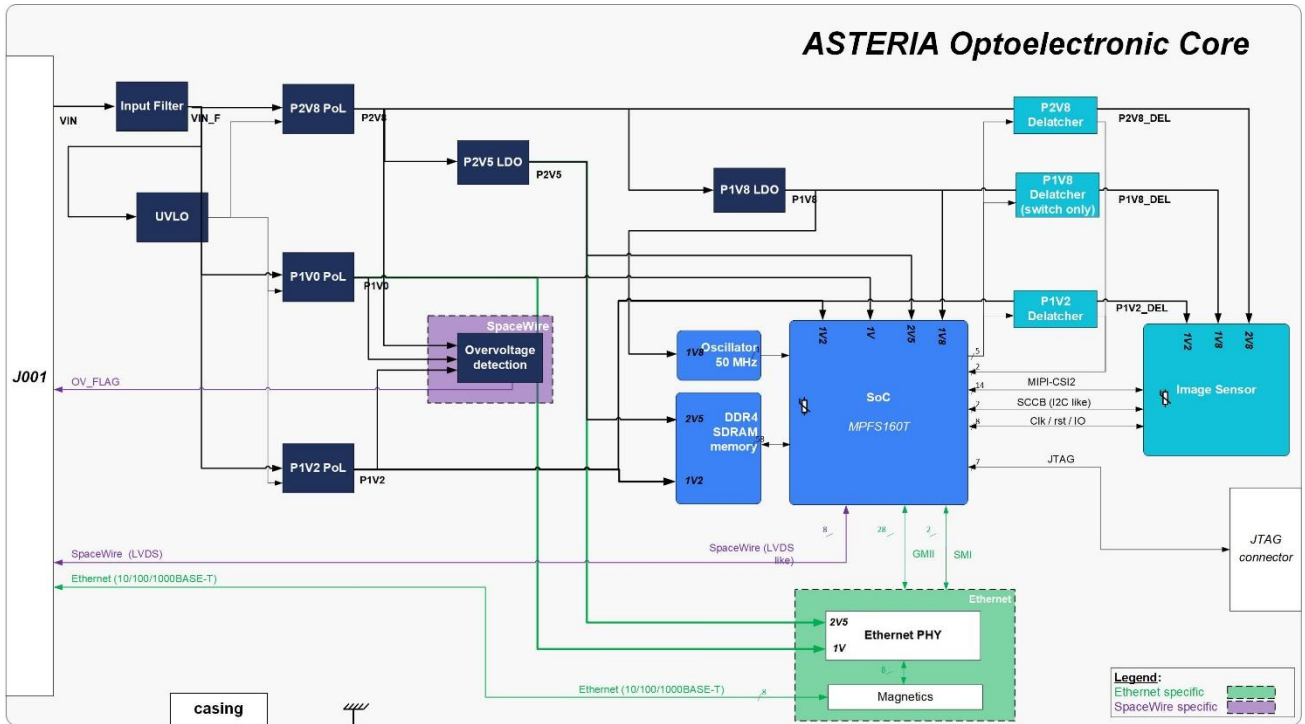


Figure 2. ASTERIA optoelectronic core architecture overview

Components Selection and Trade-Offs

The components selection was driven by a system-level trade-off between imaging and processing performance, radiation tolerance, component compactness, and long-term architecture flexibility. Beyond their individual electrical characteristics, the selected components had to be compatible with the targeted space environment while contributing to the miniaturization of the optoelectronic core.

Radiation tolerance was considered as a key selection criterion from the early stages of the architecture definition. Where available, particular attention was paid to the capability of the selected components to withstand the expected Total Ionizing Dose (TID) and Single Event Effects (SEE) environment. The target radiation robustness for the main components was a TID tolerance of at least 50 krad(Si), together with sufficient immunity to single-event latch-up for the expected Linear Energy Transfer (LET) environment, with a target SEL immunity above 60 MeV.cm²/mg. These criteria were considered together with global radiation performance including drifts and availability, maturity, and available radiation data. Extensive radiation campaigns have been performed on multiple components when radiation data was not available, especially for the image sensor. Results of these campaigns are being processed to this day for some of the components.

Compactness was another major driver of the component selection. The dimensions of the image sensor and processing device directly impact the achievable size of the 3D integrated optoelectronic core. Components were therefore selected not only according to their performance, but also according to their package dimensions and suitability for high-density three-dimensional integration.

The selected image sensor combines a high-resolution color imaging capability with a particularly compact optical format, packaged in a footprint of approximately 9 × 6.5 mm². This compact package is a significant contributor to the miniaturization of the camera and enables the optical and optoelectronic assemblies to be integrated within the targeted volume. The main trade-off associated with this selection is the use of an integrated Bayer color filter, which restricts the sensor configuration to RGB imaging. Nevertheless, this limitation is compatible with the primary ASTERIA target applications and provides a suitable compromise between imaging performance, compactness, and integration.

The processing architecture is based on a PolarFire SoC implemented in an FCSG package. The selected package provides a compact footprint while offering a scalable platform for future developments with high level of processing power

available with limited power consumption. In particular, the FCSG package family allows potential evolution toward devices with increased FPGA matrix resources while maintaining the same package footprint. This provides additional flexibility for future versions of the optoelectronic core without requiring a complete redesign of its mechanical integration.

The selected PolarFire SoC also provides an additional risk-mitigation path during the qualification process. Should the selected commercial-grade or initial device configuration not meet the final qualification requirements, migration to the corresponding radiation-tolerant (RT) version can be considered, although impacting the optoelectronic core layout, but allowing to keep most of the existing architecture. This approach reduces the potential impact of component qualification outcomes on the overall mechanical and optoelectronic design.

Overall, the component selection was therefore performed with the objective of maximizing the performance and radiation robustness available within a highly constrained physical envelope. The resulting component set provides the basis for the three-dimensional integration of the ASTERIA optoelectronic core, while retaining a degree of scalability and mitigation against component-level qualification risks.

Optoelectronic Core Integration Strategy

A key aspect of the ASTERIA development is the integration of the optoelectronic core using 3D PLUS module technology [3]. Rather than implementing the electronics as a conventional planar PCB assembly, the different electronic functions are integrated within a compact three-dimensional module, allowing the available volume to be used more efficiently as shown in the figure below.

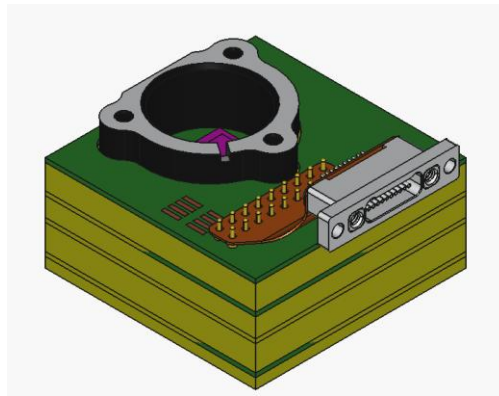


Figure 3. ASTERIA optoelectronic core 3D module integration, fitted with flex-rig PCB connector.

The ASTERIA optoelectronic core is integrated with a four-level PCB stack optimized to accommodate the different functional blocks of the camera. The four levels are organized according to their primary functions: the connector level on the top side, the image sensor level as the second level, the power management level as the third level, and the processing level at the bottom of the module.

This functional partitioning was defined to optimize both the electrical interconnections and the mechanical and thermal integration of the core. In particular, the processing level groups the processing core and DDR4 memory on the same PCB level. This arrangement minimizes the interconnection length between the processor and memory and allows the memory interface to be optimized for the high data rates required by the imaging architecture.

The processing core is located on the bottom level of the module. Its package is based on a flip-chip architecture with the silicon substrate exposed on the bottom side, providing a direct thermal interface toward the camera housing. A dedicated thermal pad is placed between the exposed package surface and the aluminium camera enclosure, providing a low-resistance thermal path for heat generated by the main processing device. This architecture enables efficient heat transfer from the SoC toward the camera structure while avoiding additional thermal components within the compact module.

The image sensor is integrated on the second level of the stack. This level incorporates a dedicated opening around the sensor to accommodate its mechanical integration with an aluminium cradle. The cradle is subsequently overmoulded

within the 3D module, providing a rigid and accurately positioned mechanical interface for the final camera integration. Its position is controlled with respect to the sensor PCB during module assembly, allowing the mechanical and optical references required for the final camera assembly to be established directly at module level.

The aluminium cradle provides both a mechanical mounting interface and an optimized optical interface with the camera optical assembly. By accurately referencing the cradle to the sensor PCB, the alignment between the image sensor and the optical system can be controlled while minimizing the number of alignment interfaces introduced during final camera integration.

The connector is implemented separately from the four-level core and is assembled after fabrication of the 3D module. A rigid-flex PCB provides electrical connection between the core and a 21-pin Nano-D connector. This approach allows the connector position and orientation to be adapted to the final camera mechanical configuration without modifying the internal architecture of the optoelectronic core. The choice of a Nano-D type of connector allows for maximum size optimization of the full camera design.

The resulting architecture combines electrical, mechanical, and thermal functions within a single highly integrated module with an overall size envelope of $30 \times 30 \times 17.2 \text{ mm}^3$. The four-level stack minimizes the required footprint while maintaining optimized interconnections between the sensor, power, processing, and memory functions. At the same time, the integration of the thermal and optical/mechanical interfaces directly into the module provides a controlled transition between the optoelectronic core and the final camera assembly, while also allowing the possibility to use it as a standalone camera head solution similar to 3D PLUS CASPEX camera heads.

The figure below shows the ASTERIA optoelectronic core stack.

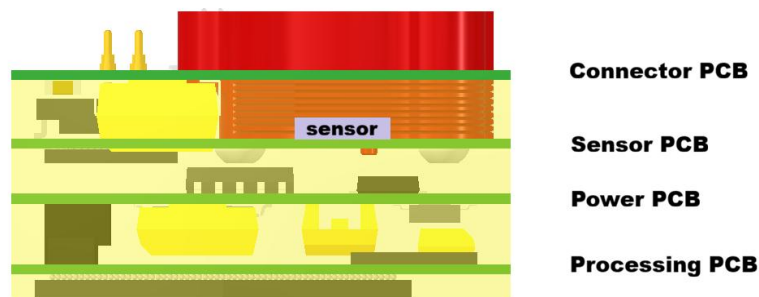


Figure 4. ASTERIA optoelectronic core stacked-up view.

3. OPTICAL AND MECHANICAL INTEGRATION

Optical Designs

To address the different imaging requirements targeted by ASTERIA, two optical configurations (medium and wide) have been developed, providing fields of view of approximately 50° and 80° , respectively. Both configurations are based on a compact seven-element optical architecture designed to be integrated with the same highly integrated optoelectronic core, while providing different levels of scene coverage.

The medium configuration provides a compromise between wide-area coverage and image sampling performance. It is primarily intended for applications requiring a relatively wide observation area while maintaining higher spatial resolution across the field. The wide configuration as shown in the figure below, targets applications requiring a larger instantaneous field of view, such as platform or payload monitoring and situational awareness. Both optical configurations were designed considering the characteristics of the selected image sensor, including its resolution and pixel pitch. Particular attention was paid to maintaining the required image quality over the complete field of view, while keeping the optical assembly compatible with the ASTERIA volume and mass constraints.

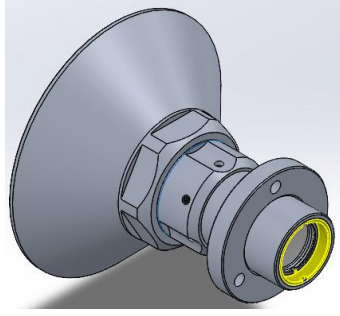


Figure 5. ASTERIA wide angle optic design, equipped with a baffle.

The main optical characteristics of the two configurations are summarized in the table below.

Table 1. ASTERIA medium and wide angle optical designs

Parameter	Medium Angle	Wide Angle
Field of View	VFoV > 28.5° HFoV > 50.0° Corners > 57.1°	VFoV > 45.9° HFoV > 80.0° Corners > 91.0°
Focal Length	8.7 mm	5.3 mm
F-number	F7.3	F7.3
Depth of Field	50cm to infinity	50cm to infinity
Distortion	VFoV < 1.4% HFoV < 4.9% Corners < 6.4%	VFoV < 4.0% HFoV < 14% Corners < 19%
Illumination Homogeneity	VFoV > 95% HFoV > 84% Corners > 79%	VFoV > 96% HFoV > 92% Corners > 91%
Transmission/ bandwidth	450-700 nm	
Glass type	Radhard Glass / Synthetic quartz	
Mass	12g (optical assembly only, without baffle)	

Mechatronic Design and Camera Integration

The mechanical architecture of ASTERIA was designed to provide a compact and mechanically robust integration of the optoelectronic core, optical assembly, and camera housing. The optoelectronic core is integrated within an aluminium enclosure that provides both mechanical protection and a defined thermal path for the main heat-generating component, the processing SoC.

A thermal interface pad is located on the bottom side of the optoelectronic core, directly below the PolarFire SoC die, and compressively held when assembled. The pad provides a low-thermal-resistance interface between the main processing device and the aluminium enclosure, enabling heat generated by the processor to be efficiently transferred toward the camera structure and subsequently dissipated to the spacecraft thermal interface.

On the top side, the optoelectronic core is mechanically constrained by the camera housing and interfaces directly with the miniaturized optical assembly through its sensor cradle. This configuration allows the optical and electronic functions to be packaged within a common compact volume while maintaining a controlled mechanical interface between the image sensor and the optical system.

The mechanical architecture was developed concurrently with the optical and electronic designs, with particular attention to the overall dimensional envelope, structural stiffness, component protection, thermal paths, and optical alignment. The resulting configuration minimizes the number of mechanical interfaces and avoids the need for a separate electronic enclosure, contributing to the overall compactness of the ASTERIA camera.

The figure below shows an overview of the ASTERIA camera assembly.

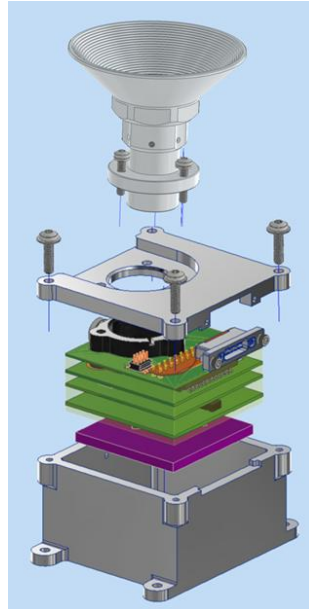


Figure 6. ASTERIA Camera full mechanical design, wide optics configuration.

The mechanical and thermal design has been assessed through preliminary structural and thermal analyses under the expected launch and operational conditions. Further optimization and experimental correlation will be performed during the prototype characterization phase. The aluminum enclosure also provides additional radiation shielding to the optoelectronics core components. Sectorial analysis using FASTRAD software has been performed to optimize the thickness of the enclosure, as well as critical component's location in the module design to allow a maximum dose seen at component level compliant with the expected radiation performances, including with radiation design margin. This work is still ongoing.

At this stage of the development, the expected envelope and mass budget for the ASTERIA camera is a volume of $41.5 \times 40 \times 43 \text{ mm}^3$, for a mass of 82g (without baffle). While including the fixation ears and the baffle, the global volume becomes $41.5 \times 48 \times 58 \text{ mm}^3$.

4. DEVELOPMENT STATUS AND REMAINING ACTIVITIES

At the time of writing, the ASTERIA development has reached a significant design and architecture validation milestone. Several key elements of the camera have already been demonstrated or completed at design level, while the manufacturing and validation phases of the prototypes are ongoing.

After assessment and selection of the components and architecture with respect to the expected performances, space radiation and temperature environment, the full optoelectronic core architecture has been implemented on a two-dimensional breadboard and functionally demonstrated, including image sensor readout at the maximum targeted frame rate, Gigabit Ethernet interface operation at maximum speed, and validation of the main power architecture.



Figure 7. ASTERIA optoelectronic core 2D breadboard (left) with image sensor daughter board (right).

The power architecture was especially assessed using representative digital design processing video stream with image processing at maximum framerate. Power consumption ranging from 3.5W at 25°C to 6W in worst case condition (SoC junction temperature > 90°C). Power optimization and thermal correlation remain ongoing activities to enhance the final design target.

The next phase of the development focuses on the transition from breadboard and design validation to the integrated camera with the first prototype batch manufacturing, intended to be submitted to full product characterization and validation, with electro-optical, functional, thermal, and interface testing of the integrated prototypes. The ongoing development of ASTERIA space grade digital design for its processing core will be included in this validation phase, as part of the full product, taking into account radiation mitigation for enhanced reliability. Flight-grade model manufacturing will follow the prototype validation and ASTERIA will be submitted to full product qualification, with regards to applicable environmental qualification activities such as thermal-vacuum, vibration, shock, and standard reliability qualification such as thermal cycling, life test and endurance cycling.

The results presented in this paper therefore represent a development milestone rather than a final qualification assessment. They demonstrate the feasibility and maturity of the main ASTERIA architectural choices, while the integrated prototype characterization and flight-grade qualification remain to be completed. Final product performance and environmental compliance will be established through the remaining activities.

5. CONCLUSION

In the framework of its R&D activities, 3D PLUS is developing the ASTERIA Space Camera to address the increasing demand for compact low-power and highly integrated imaging systems. Driven by a set of demanding requirements that led to a system-level trade-off between component performance, processing capabilities, interfaces, integration, and overall SWaP-C aspect, a highly integrated optoelectronic core is being developed and demonstrated as the central element of the ASTERIA architecture. This development is done together with a compact optical design and an integrated optomechanical architecture allowing 3D PLUS to provide a miniaturized and flexible imaging solution suitable for the future monitoring camera needs of space exploration.

At the current stage, the main architecture has been demonstrated on a 2D breadboard, including sensor acquisition, high-speed Ethernet communication, and representative image processing. Radiation analyses, optical design, and preliminary structural and thermal analyses have also been performed. The first prototype batch is currently being manufactured and will enable the characterization and validation of the integrated camera. Prototypes of ASTERIA are expected during the first half of 2027. Qualification and full flight grade ASTERIA cameras are expected for early 2028.

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