

Teledyne e2v technology developments: HiRho pixel and TDI

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ABSTRACT

Teledyne e2v develops silicon sensors for ground and space-based applications. Two technology developments are going to be presented, updates on HiRho pixel operation, and new TDI developments.

The HiRho technology helps sensors enhance their Near-Infra-Red performance. The production of the sensor on a thicker epi helps with the QE, but the MTF is maintained, or even improved thanks to the full depletion of the silicon substrate, due to the backbias voltage. This technology has been implemented in CIS304 (a generic multi-purpose detector 4.5k x 4.3k 10µm pixel pitch, 5T pixel with selectable dual gain and selectable global and rolling shutter operation), which has been selected for the Arrakis mission with ESA. Results of the testing of this sensor operating at 200K will be presented, demonstrating the performance of this technology at low temperatures.

Teledyne e2v has developed testchips demonstrating the CCDonCMOS technology, and has developed sensors utilising this technology in TDI sensors, like CIS125 (a generic TDI sensor providing 4 dual PAN bands with 5µm pixel pitch and up to 6 MS bands with 10µm pixel pitch, operating at 14kL/s). Recently we tested the silicon at a different operating condition (low temperature and reduced biases), maintaining good CTE without changing the design. These results will be presented.

Keywords: CMOS, HiRho, low temperature, TDI, CCDonCMOS

1. INTRODUCTION

Space imaging is experiencing a rapid growth, especially in New Space markets where the detectors are at the centre of many systems. This growth takes advantage of the advances in commercial technology to enable more complex missions with better return on investment. This also leads to existing technologies and image sensors being used in specialized conditions (environmental or others).

The route to support this evolution is to widen and strengthen the characterization of the devices employing existing technology under new mission conditions. Teledyne-e2v presents the results covering the latest measurements for HiRho and CCDonCMOS.

Performance results on the low temperature operation of the CIS304 sensor will be presented. CIS304 is a generic multi-purpose detector 4.5k x 4.3k 10µm pixel pitch, 5T pixel with selectable dual gain and selectable global and rolling shutter operation. This testing proves the operation of HiRho technology at near-cryogenic temperatures which allows this sensor to be used in high performance applications such as those planned for the ESA Arrakis instrument.

A new condition for the CCDonCMOS technology will be presented. The technology has been utilised by Teledyne in the development of TDI sensors, for example the CIS125 which is a generic TDI sensor providing 4 dual PAN bands with 5µm pixel pitch and up to 6 MS bands with 10µm pixel pitch, operating at 14kL/s. The focus of this testing is low temperature operation of the existing design. Characterisation results will be presented for this test, focusing on Dark Signal and CTE.

2. CIS304 DETECTOR

Teledyne e2v designed a general purpose large area CMOS sensor, the CIS300 and variants of it. A member of that family, CIS304, which had been designed by Teledyne, was proposed as one of the Visible Image Sensors for the Arrakis mission. This chapter acts as an introduction.

2.1 CIS304 Detector details

The CIS304 is a flexible large area detector platform. [1] It is built in a stitched format, and the size selected here features:

- 4,500 columns and 4,340 rows of $10\mu\text{m} \times 10\mu\text{m}$, selectable dual gain pixels
- Capable of rolling shutter, global shutter and High Dynamic Range (HDR) Operation
- Selectable 12 bit or 14 bit operation (effectively extendable by HDR)
- High frame rates from 6 CML outputs each running at 2Gbit/s
- Region Of Interest (ROI) feature enabling fast access to small pixel areas of interest
- High quantum efficiency (QE) from Teledyne's world leading backthinning processing
- Designed for use over a wide range of temperatures - room to cryogenic temperature
- Enhanced near infrared performance while maintaining high modulation transfer function (MTF) performance thanks to implementation of HiRho technology.

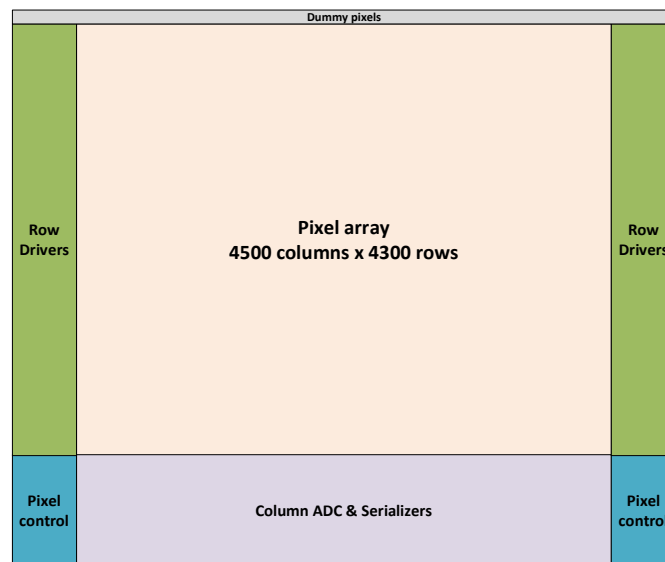


Figure 1 View of the CIS304 floorplan

Finally the package for the CIS304 is the standard package for the CIS300 family and can be seen in Figure 2.

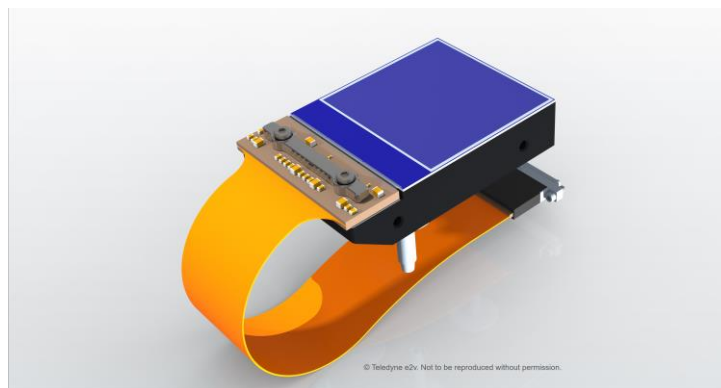


Figure 2 CIS304 detector

This package was designed to be 3-side buttable.

- <1mm dead space between image area and adjacent package surfaces on the 3 close-butting sides.

- 2 mm dead space between adjacent image areas on a Focal Plane Array arrangement
- Designed to operate at temperatures from 180-313K
- Image area flatness per sensor < 25 μm typical peak-to-valley (based on the distance between two closest parallel planes that encompass the full image area.)

Height tolerance per sensor of $\pm 20 \mu\text{m}$ through use of precision shims (based on variation between best fit image area plane and best fit plane between the 3 shim interface surfaces)

2.2 ARRAKIHS Mission details

Analysis of Resolved Remnants of Accreted galaxies as a Key Instrument for Halo Surveys (ARRAKIHS) is an ESA mission designed to address a central Cosmic Vision question: how galaxies assemble their mass and structure through hierarchical accretion. By targeting the extremely faint stellar outskirts of nearby galaxies, Arrakihs will provide the first statistically robust and homogeneous census of stellar halos and low-surface-brightness features (LSBFs) around Milky Way-mass galaxies beyond the Local Group. [2]

ARRAKIHS is an ESA mission, with the Arrakihs Mission Consortium (AMC) serving as the international partnership responsible for the mission's science, payload (science instrument), Instrument Operations and Science Data Centre (IOSDC), and scientific data exploitation. The current goal is to launch into a low-Earth, sun-synchronous orbit around end of 2030.

The 4 detectors integrated in the satellite will offer the following filter responses.

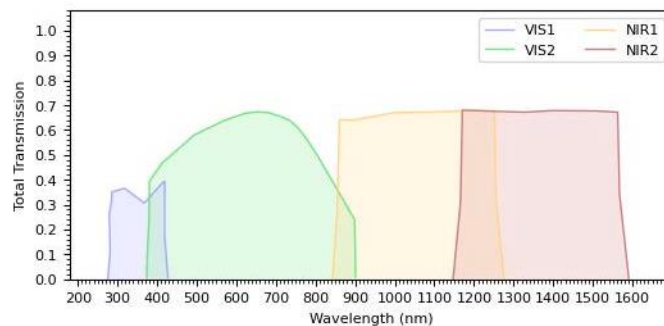


Figure 3 ARRAKIHS instrument filter responses corresponding to the respective channels [2]

3. HIRHO AT LOW TEMPERATURES

3.1 HiRho Technology basics

In CMOS technology, the photodiode depletion depth is smaller in comparison to the CCD. This is due to the fact that CMOS uses lower voltages. This lack of deep depletion implies that once back thinned the total thickness cannot exceed around $10\mu\text{m}$ without a strong MTF degradation. This limits the QE in NIR. The HiRho technology addresses this dilemma. This technology consists of supplying a negative voltage, named reverse bias, to the back surface while preventing the transistor from leaking [3]. Figure 4 shows a representation where the Deep Depletion Extension (DDE) is a special implant added in the pixel to protect the in-pixel transistors from the reverse bias.

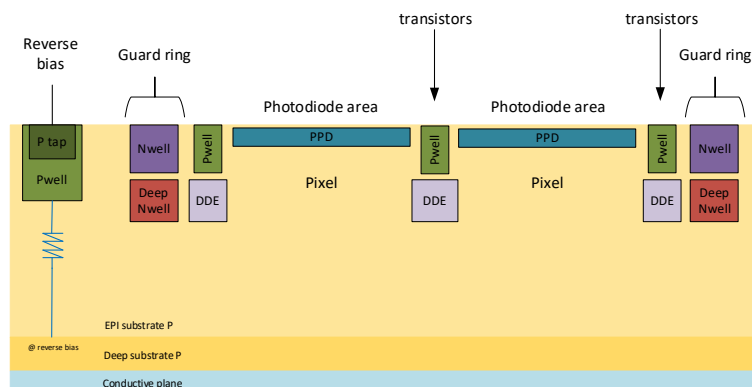


Figure 4: HiRho – 2 pixels reverse bias in-pixel DDE protection representation.

This technology has been implemented successfully as part of a European Space Agency GSTP funded program. The device CIS220 which is being considered for ESA's LISA mission (LISA [Laser Interferometer Space Antenna] will be the first space-based observatory dedicated to studying gravitational waves [4]) was the first to implement and demonstrate the technology. It is the HiRho version of CIS120, a generic multi-purpose detector 2k x 2k 10 μ m 5T pixel pitch global and rolling shutter operation (which has been selected for Copernicus missions). The QE and MTF have been measured for two EPI thicknesses of 17 μ m with -6V reverse bias, and 33 μ m with -20V reverse bias, see Figure 5 and Figure 6. The MTF is almost a constant across the wavelength which demonstrates full depletion, although the values are slightly lower than the perfect theoretical value and slightly lower for the 33 μ m thickness compared to 17 μ m. This is explained by the aspect ratio between the pixel pitch 10 μ m and the thicknesses (17 μ m and 33 μ m). Some electrons due to the lateral diffusion effects happening close to the back surface can escape the pixel depletion region to be captured by a neighbouring pixel. Nevertheless, these results show an important sensitivity increase in the NIR compared to the CIS120 non-HiRho detector. The QE response of CIS220 is significantly higher from 700nm and almost double from 850nm onwards for the 33 μ m compared to the CIS120. Importantly MTF performance of the CIS220 is not compromised by using thicker silicon and is improved compared to CIS120. It is worth pointing out that as the QE roll off appears later, the fringing effect is reduced improving drastically performance for narrow wavelength bandwidth applications like hyperspectral. This is another important key point of this technology.

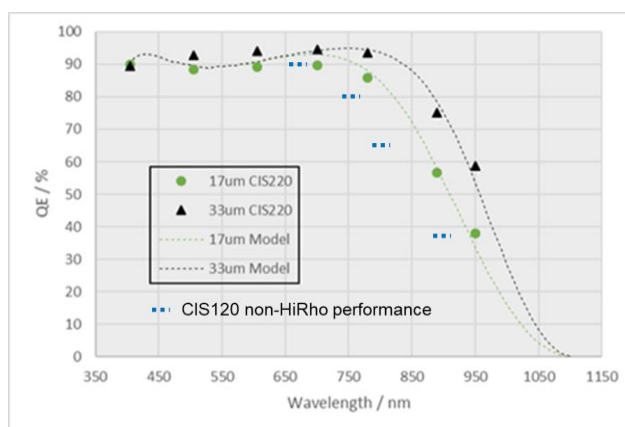


Figure 5: CIS220 HiRho QE response for two thicknesses and comparison with non-HiRho CIS120 thinned to 9 μ m.

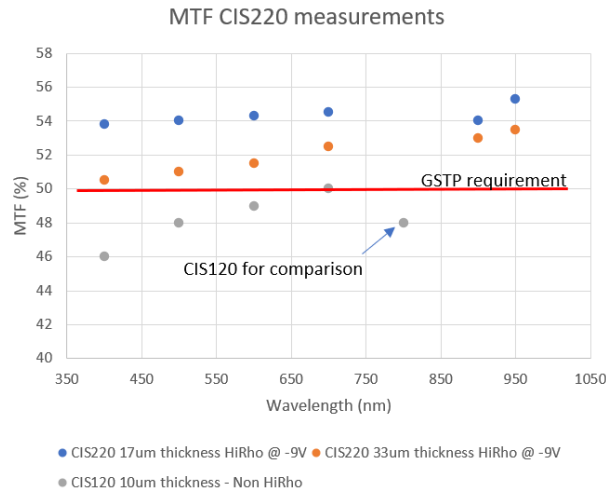


Figure 6: CIS220 HiRho MTF response for two thicknesses.

3.2 HiRho sensor behaviour Room vs Low Temperature

CIS304 is a sensor that is HiRho and has been tested at room temperature and also at 200K (or -73oC as mentioned in multiple graphs in this chapter). This testing shows that HiRho performance remains unaffected at low temperatures.

3.2.1 Leakage Current

The front to back (i.e. VBB or Voltage BackBias to ground) leakage current has a strong dependence on the temperature. With colder temperatures, there is less thermal energy, fewer free carriers, so the knee points moves to higher absolute voltages (more negative- see Figure 7). It remains possible to select a good VBB for both temperature scenarios- the optimum may be different, but operation can be maintained across temperatures.

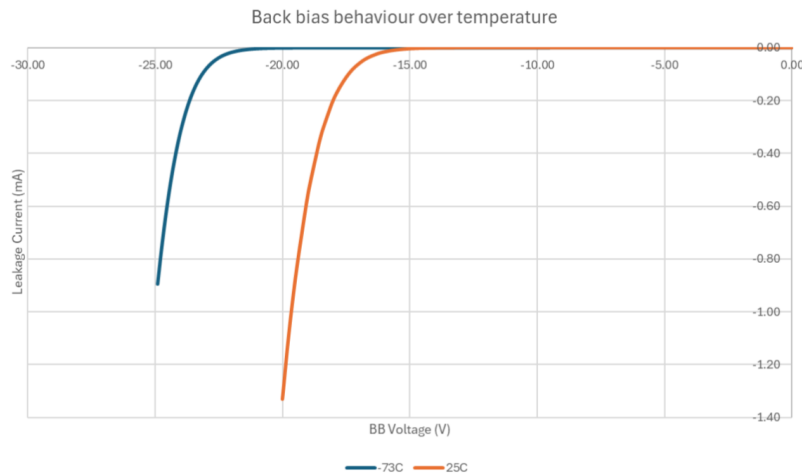


Figure 7 Leakage Current over temperature

3.2.2 EO performance

The performance of key parameters in rolling shutter operation in both High Full Well (HFW) and Low Full Well (LFW) modes are shown in Table 1. The pixel can alternate between the two modes by utilising an optional large capacitor added to the Sense Node (SN) capacitance.

		25°C	-73°C	Units
HFW	CCF	0.07	0.07	ADU/e-
	Qsat	76.9	69.2	Ke-
	Qlin	67.7	59.7	Ke-
LFW	CCF	0.70	0.72	ADU/e-
	Qsat	18.5	17.7	Ke-
	Qlin	17.0	17.0	Ke-
HFW	Noise	23.9	20.0	e-
LFW	Noise	5.3	2.3	e-

Table 1 Table of key EO data at different temperatures

Explanation of parameters:

CCF=Charge to Code Factor (provides Analogue to Digital Units)

Qsat=photogenerated Charge at Saturation point

Qlin= photogenerated Charge at maximum Linear point

CCF, Qsat and Qlin show negligible change with temperature. Noise shows a reduction with temperature as expected. The measured noise includes dark signal contribution, as the frame rate is not high, which leads to a reduction at low temperature where lower dark signal is present. Many contributors to the electrical readout noise also reduce with temperature, as simulation predictions of the electrical behaviour showed, due to their thermal nature. This statement holds for parts of the Source Follower, Column Current, Analogue to Digital Converter and sampling/kTC noise.

Also it is noted that power consumption changes:

	+25°C	-73°C
Power Consumption (W)	2.43	2.54

Table 2 Power consumption over temperature.

Power consumption increases by 4.5% at -73oC versus 25oC.

This is no surprise, because of the huge digital operation that dominates the power consumption of CIS304. While at low temperatures the current through each individual transistor drops (due to the relationship of transistor current vs temperature), this implies that there is less current in digital gates to help them switch, so the switching happens a bit slower. This means the transition from low to high or high to low (zero to one or one to zero) takes longer, and the shoot through current that occurs during the transition goes up. This generally is expected to slightly increase the power consumption at lower temperatures.

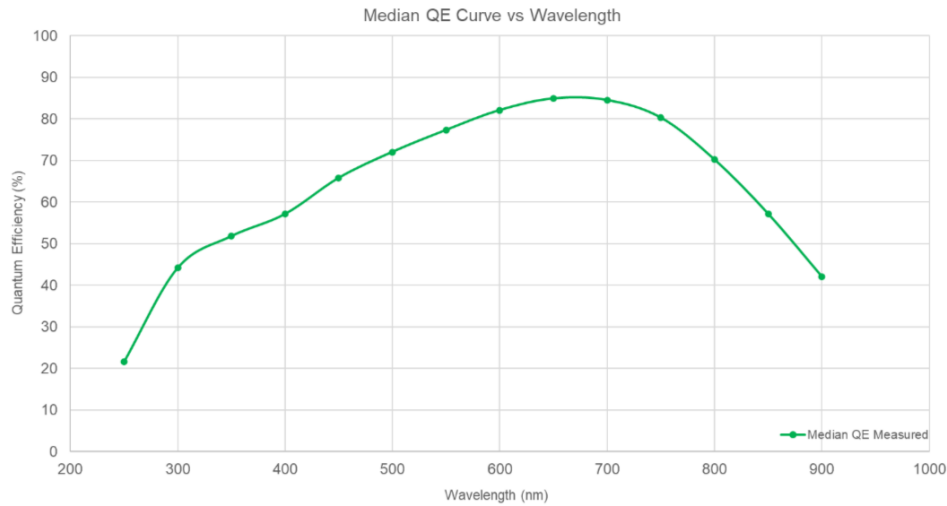


Figure 8 QE measured at 200K

The QE behaviour is shown in Figure 8. Performance remains improved at NIR wavelengths up to 900nm thanks to the thickness of the backthinned silicon (20 μ m) even at low temperatures.

3.2.3 Image sharpness

The image sharpness is measured by the steepness of the transition between dark and bright regions illuminated through a mask on top of the image array. The results include some proportion of optical cross-talk or spread.

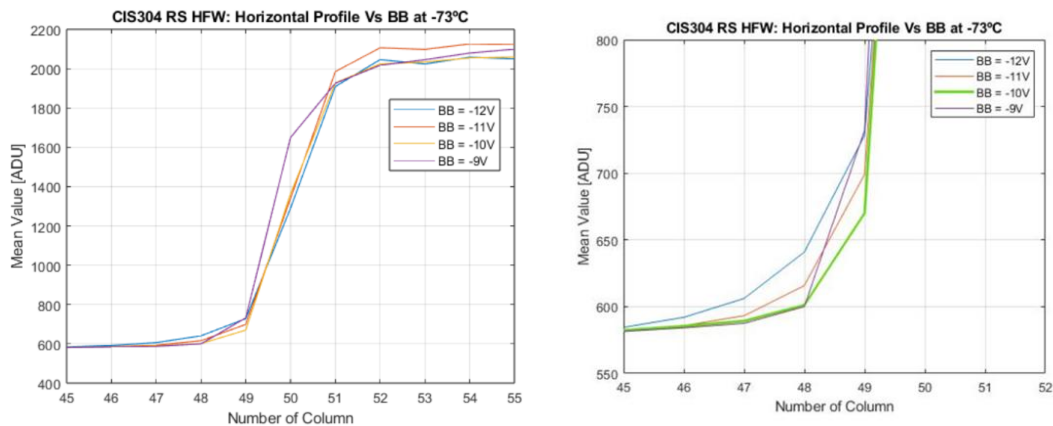


Figure 9 Edge behaviour over different VBB full scale (left) and zoomed in (right).

A sharp transition can be observed at low temperatures, and in Figure 9 it can be seen that based on the choice of backbias voltage (VBB) image sharpness can be optimized and transition can be made sharper (see section 3.2.1 for VBB across temperature).

3.2.4 Dark Signal and Glow

Measuring dark signal (DS) at low temperatures at nominal fast frame rates has the complication that the amount of DS is very low. Therefore the measurement is required to integrate for a prolonged duration. This has the consequence that we capture glow from the readout, which artificially increases the average dark signal measured.

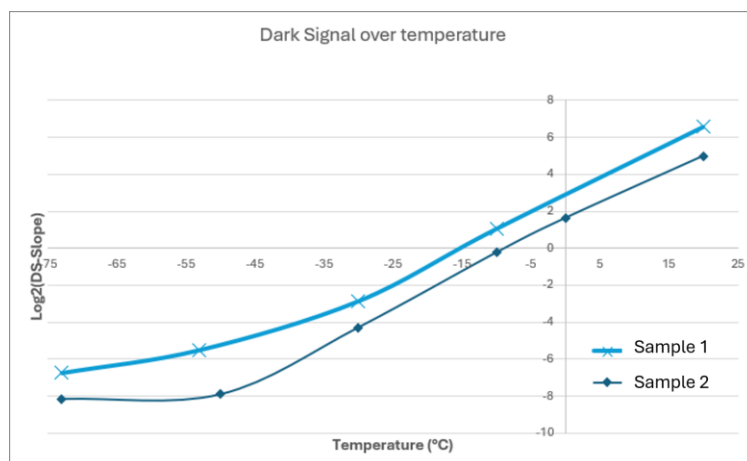


Figure 10 Image area average DS vs temperature for two samples

The measured DS follows the expected reduction in Dark Signal (DS) with lower temperature, until the point where the results seem to plateau, at low temperatures because of glow. Dark signal is measured to double every 5.24oC, which is in line with expectations for a doubling factor.

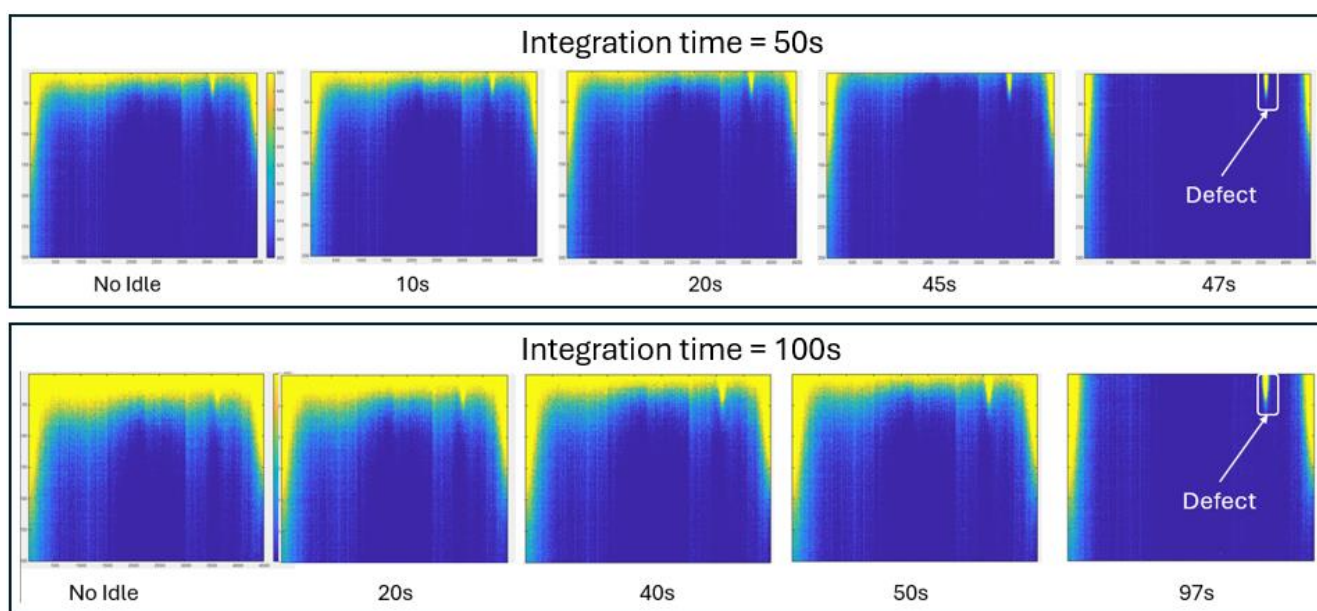


Figure 11 Glow over different integration durations with idle enabled

For Figure 11 the readout is on the top, which seems to be the source of glow, including some defects.

The sensor is designed with the ability to enable a low power operation (idle mode), where the readout consumes less and thus glows less. This ability can be seen here, staying in idle for most of the integration duration clearly helps reduce the amount of glow observed.

4. TDI CHARGE DOMAIN

Teledyne's TDI heritage has been built on test results from silicon that proved the CCDonCMOS technology, and products that used it like CIS125. In the interest of potential future missions with ESA it was important to understand the behaviour of TDI at low temperatures. A dedicated characterization activity, using the testchip for TDI (CIS123) was completed, and the results are summarised in this section. The device used for these measurements (CIS123) was started under a CEOI EO technology and Instrumentation program, funded by the UK Space Agency. [5]

4.1 TDI basics

The pixel, Figure 12, is a CCD structure, with gated anti-blooming (AB), implemented in CMOS technology. The charge is integrated while moving within the silicon, by pulsing the Phase Clocks sequentially (shown as P1 P2 P3 P4), so we achieve TDI (time delay integration). The interface of this structure to the readout resembles a classic CMOS pixel with a Source Follower and the Column Readout following on.

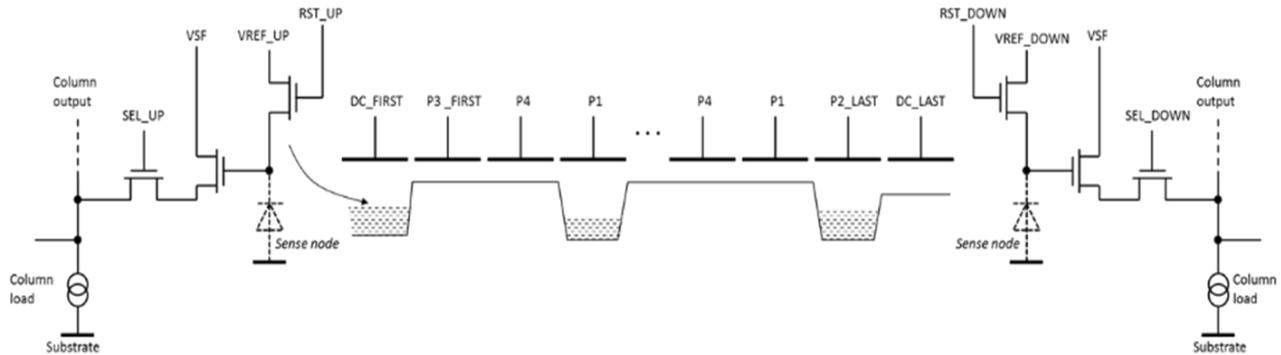


Figure 12: TDI Pixel schematic (CCDonCMOS)

A key parameter for such technology is the Charge Transfer Inefficiency (CTI) performance. This in turn determines the maximum FWC of the pixel before the pixel change from a buried regime to a surface regime. The latter is usually not preferred due to possible degradation of the MTF performance. This is not the case for a pixel working in buried mode only.

The CIS123 silicon includes both 5 μm and 7 μm pixel. The results of the CTI versus signal curves indicated the associated FWC by an abrupt increase in CTI when the charge reaches the surface. The CTI and FWC obtained on both the 5 μm and 7 μm pixel pitch of the back illuminated test chip version are shown in Figure 13. The FWC is clearly improved with higher CLK_HIGH bias- reaching 30ke- for 5 μm under appropriate bias.

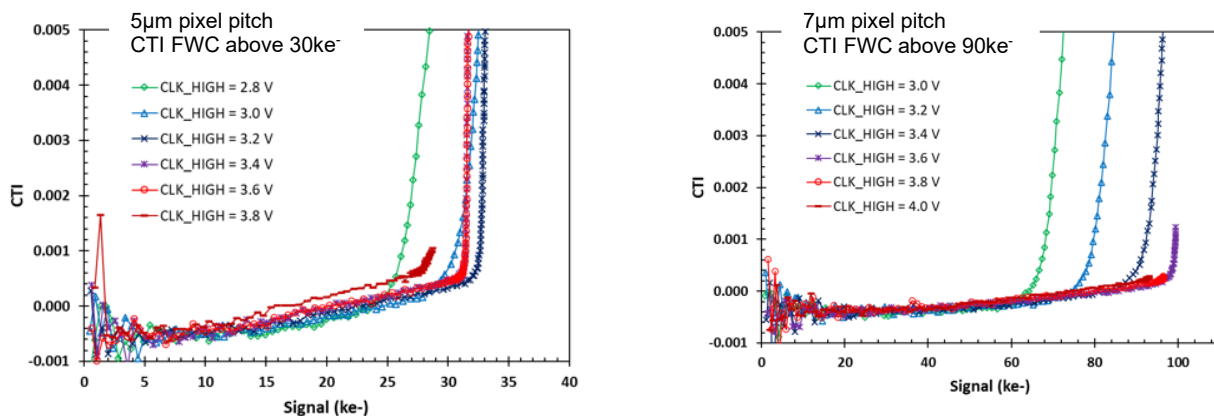


Figure 13: CTI and FWC associated for 5 μm pixel pitch (left) and 7 μm pixel pitch (right) at room temperature.

4.2 TDI measurements at low temperatures

A characterisation activity was performed using the CIS123 TDI pixel test chip and with the TDI design unchanged. The focus is on the performance at low temperature of two interconnected parameters, CTI and Dark Current. The parameters are measured versus signal level and clock voltages.

4.2.1 Dark Current

Dark Current has is shown to have a direct relationship to clock high amplitude, with reducing clock amplitude reducing the measured dark current.

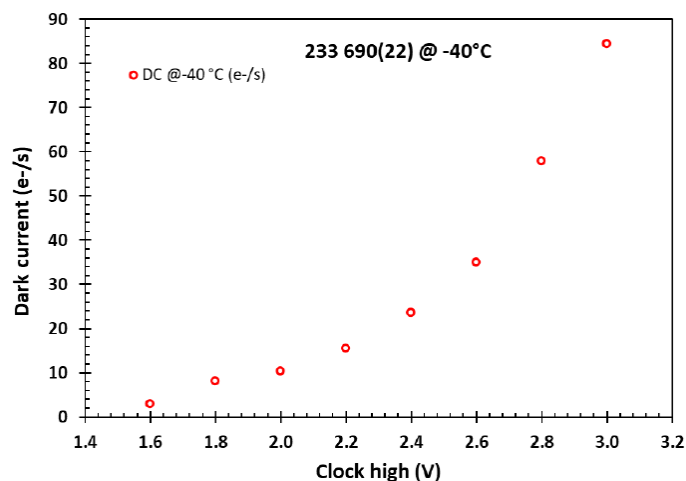


Figure 14 Relationship between Dark Current and Clock High [6]

For the above test, Clock Low was kept the same for fair comparison and the temperature was kept at -40oC.

The behaviour of Dark Current over temperature was measured and found to follow the expected Arrhenius relationship with temperature. The results show an activation energy of traps and defects very close to half the natural bandgap energy of silicon as expected

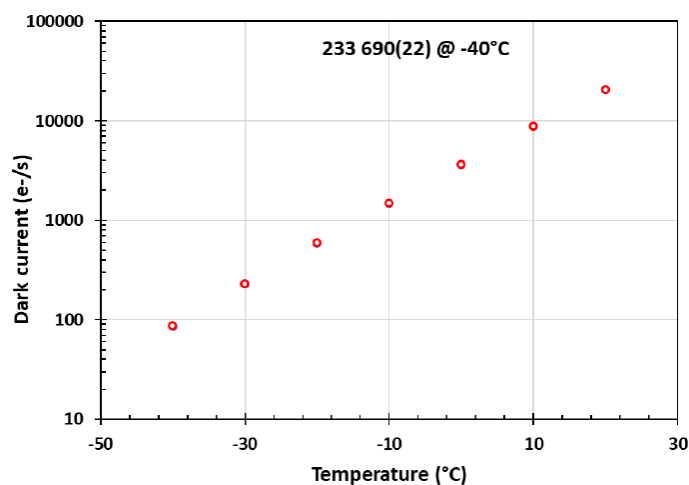


Figure 15 Dark Current over temperature. [6]

4.2.2 Charge Transfer Inefficiency (CTI)

For measuring CTI, it is acknowledged that the test method creates consistently negative results for mid-level amounts of charge. This is considered not real but an artefact of the measurement.

CTI when measured at -40oC and it looks similar to the room temperature measurement (Figure 16 can be compared to Figure 13)

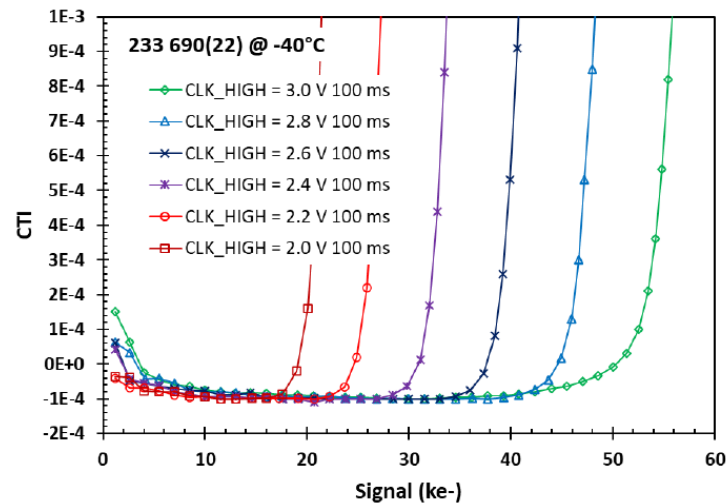


Figure 16 CTI against signal level for various CLK_HIGH values [6]

The low signal end of the CTI plot is shown in Figure 17. This shows that CTI is lower for lower CLK_HIGH bias. This is the same trends as for the dark signal findings of section 4.2.1.

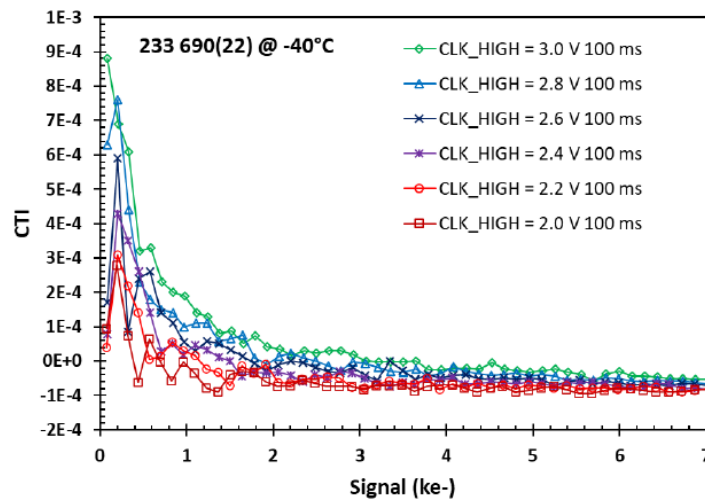


Figure 17 CTI against low signal, for various CLK_HIGH [6]

The above finding was validated both with other low temperatures (tests were repeated for -30oC and -20oC), and other test methods- specifically Fe55 was used to get around the negative values.

These results show that using the existing TDI pixel design from Teledyne with modified operating conditions, namely reducing the clock high voltages while operating at low temperatures, improved CTI and dark signal performance can be achieved. This enables the pixel design to be baselined for use in new applications.

5. CONCLUSIONS

The expanded use of existing CMOS pixel technologies has been demonstrated through characterization testing.

Performance of HiRho technology at 200K has been demonstrated by means of test results for the CIS304, which is a generic multi-purpose detector 4.5k x 4.3k 10µm pixel pitch, 5T pixel with selectable dual gain and selectable global and rolling shutter operation. The operation of HiRho at cryogenic temperatures has been shown to not be significantly impacted compared the room temperature measurements, with a decrease in read noise and only a minor increase in power dissipation.

CCDonCMOS TDI pixel technology performance testing aimed at low temperature conditions was conducted. The results show good CTI and low dark signal at low temperatures if clock high biases are reduced. These results create the confidence that the technology as implemented in existing Teledyne silicon can be used in a wider range of applications.

Characterisation of existing technologies and sensors in novel conditions will keep creating new opportunities for re-use and is a means of reducing risk for new missions and helping with securing the timescales.

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