

120 Gb/s BGA-solderable VCSEL transceiver engine enabling near-package optics for intra-satellite optical interconnects

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ABSTRACT

We present a VCSEL optical transceiver (OTRx) engine for near-package intra-satellite interconnects that provides a 4×30 Gb/s (120 Gb/s aggregate) data rate and can be directly soldered to a host PCB through a BGA interface. The $17.6 \times 19.2 \times 2.84$ mm package integrates four transmit and four receive optical channels at 850 nm, based on GaAs VCSEL and photodiode quad arrays, together with the corresponding radiation-hard electronic front ends comprising a quad VCSEL driver and a quad transimpedance amplifier IC. All chips are assembled by flip-chip bonding on a single-layer transparent glass chip carrier (TGCC). A molded optical coupling unit provides beam collimation, light turning and focusing, with guide-pin alignment to a removable MT ferrule. The TGCC is bonded on a high-thermal-conductivity ceramic package that implements the electronic fan-out. The ceramic package hosts the BGA interface that enables reflow of 160 SnBiAg solder balls of 300 μ m diameter directly onto an evaluation PCB. X-ray verification and post-reflow testing confirmed the supply, control high-speed signal paths. The OTRx achieves back-to-back, error free ($\text{BER} < 10^{-12}$) operation at 30 Gb/s with 5 dB transmitter extinction ratio and over 1 mW optical output power, while eliminating the use of external LGA interposer or socket; demonstrating solder-reflowable near-package optical I/O for high-speed intra-satellite links.

Keywords: VCSEL, optical transceiver, intra-satellite interconnect, near-package optics, SiGe BiCMOS, radiation-hard electronics, BGA, solder reflow

1. INTRODUCTION

The continuing growth of digital payload processing, high-resolution sensing and on-board data handling is increasing the number and rate of high-speed serial links inside satellites. Fiber-optic interconnects are attractive because they can provide high aggregate bandwidth with low cable mass and immunity to electromagnetic interference while decoupling link reach from the loss and equalization constraints of high-speed copper channels. VCSEL-based intra-satellite links have been investigated for nearly two decades before the successful deployment of 10 Gb/s optical interconnects in a commercial mission [1].

More recent roadmaps have moved toward parallel, board-mounted optics at lane rates above 20 Gb/s [2]. Board-mountable VCSEL transceivers operating at >25 Gb/s were demonstrated as research prototypes [3] as well as commercial products [4] while a 112 Gb/s radiation-hardened mid-board optical transceiver architecture based on 130-nm SiGe BiCMOS driver and receiver ICs was reported in [5]. Subsequent work demonstrated an integrated radiation-hard VCSEL-driver/TIA chipset and optical module for on-board satellite interconnects [6] and end-user studies have confirmed the migration of digital transparent processors toward optical links above 20 Gb/s [2]. In parallel, co-packaged-optics concepts using radiation-hardened electronics and silicon photonics are being investigated for future satellite payloads [7].

These developments establish the benefit of moving the electrical-to-optical conversion progressively closer to the high-throughput host ASIC or FPGA. However, conventional mid-board implementations typically retain a pluggable high-speed electrical connector, socket or interposer between the optical module and the host PCB. For near-package optics (NPO), this interface becomes increasingly important because it contributes to electrical loss, mass, package height, thermal resistance and eventually procurement and qualification cost. The OTRx presented in this paper addresses this packaging constraint by treating the optical engine as a surface-mount BGA component that can be soldered directly onto the host board, while retaining a removable multi-fiber optical connector.

Our OTRx architecture combines GaAs VCSEL and PIN-photodiode arrays, radiation-hard SiGe BiCMOS electronic ICs, a transparent glass chip carrier, passive molded micro-optics and a high-thermal-conductivity ceramic package. The

VCSEL-driver and TIA ICs have been fabricated through a rad-hard 130 nm BiCMOS process and have been reported in [8] and [9]. The present paper focuses on the complete optical engine architecture, packaging, board-level assembly and functional characterization performed after solder reflow on a host board. The key contribution is a compact 4-Tx/4-Rx optical engine that replaces the external high-speed electrical interposer with a direct 160-ball BGA interface and demonstrates 30 Gb/s-per-lane operation.

2. OPTICAL TRANSCEIVER ARCHITECTURE

2.1 Functional architecture

Figure 1 shows the OTRx functional diagram. The transmitter path contains a four-channel VCSEL-driver IC connected to a 1×4 VCSEL array, while the receiver path contains a 1×4 PIN photodiode array connected to a four-channel transimpedance-amplifier (TIA) IC. Both electronic ICs include SPI interfaces for configuration, monitoring and control. Four differential electrical inputs and four differential electrical outputs are routed through the BGA package to the host board, while the optical interface is provided by a removable multi-fiber MT connector. Table 1 summarizes the target OTRx design specification.

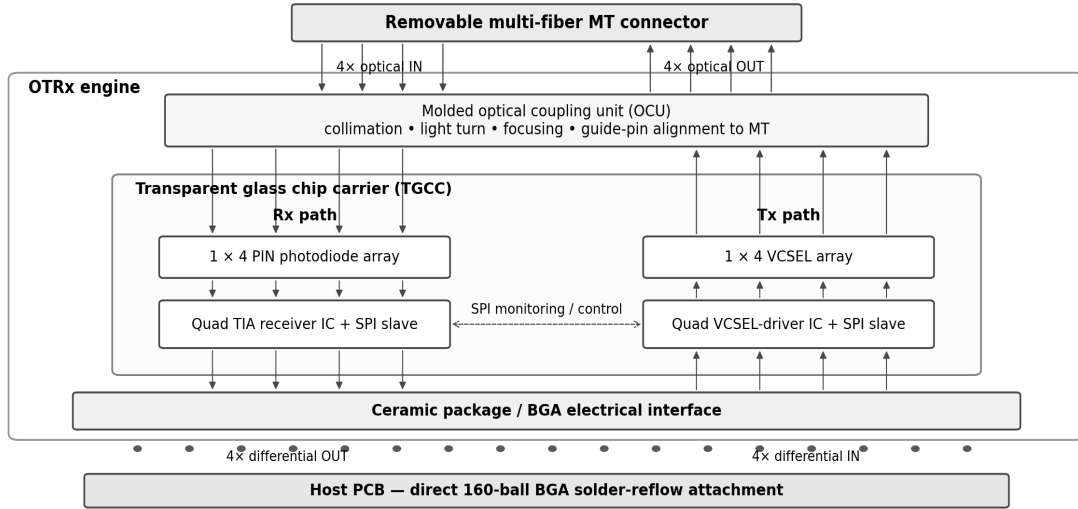


Figure 1. Functional architecture of the optical transceiver engine, showing the four-channel transmitter and receiver paths, SPI control interfaces, BGA electrical interface, optical coupling unit and removable MT connector.

Table 1. OTRx functional design specification

Parameter	Target / nominal value
Operating wavelength	850 nm
Number of channels	4 Tx + 4 Rx
Signaling rate	30 Gb/s per lane, NRZ OOK
Typical launch optical power	≥ 0 dBm per Tx lane at room temperature
Extinction ratio	≥ 3 dB at room temperature
Optical modulation amplitude	≥ -1.76 dBm for ER = 3 dB
Supply voltages	3.3 V Tx / 2.5 V Rx
Total power efficiency (Tx + Rx @ 120Gb/s)	4.8 mW/Gb/s
Typical Differential input swing	600 mVpp
Typical Differential output swing	300 mVpp

2.2 Package stack-up and optical interface

The assembly design including the mechanical and optoelectronic components is shown in Fig. 2. The central element is a transparent glass chip carrier (TGCC). The VCSEL array, photodiode array, VCSEL-driver IC and TIA IC are flip-chip bonded on the metal side of this carrier (the metal layer and the glass substrate are shown separately in the figure). The

optical beams propagate through the glass to reach the optical coupling unit, which is mounted on the opposite side. This vertical arrangement separates the optical connector interface from the active-die side, while maintaining short electrical interconnects between the optoelectronic arrays and the corresponding electronic ICs.

The molded optical coupling unit (OCU) is made of a temperature resistant thermo-plastic and hosts the micro-optics required for beam collimation, light turning and focusing. Mechanical guide pins on the OCU engage the alignment holes of the MT ferrule, providing passive alignment of the removable connector to the optical fibers. The MT connector can therefore be mated independently. The TGCC/OCU subassembly is mounted on to the ceramic package, which is designed with an appropriately sized cavity to fit with the protruding chips. thus protecting the active components and providing the BGA electrical interface to the host board.

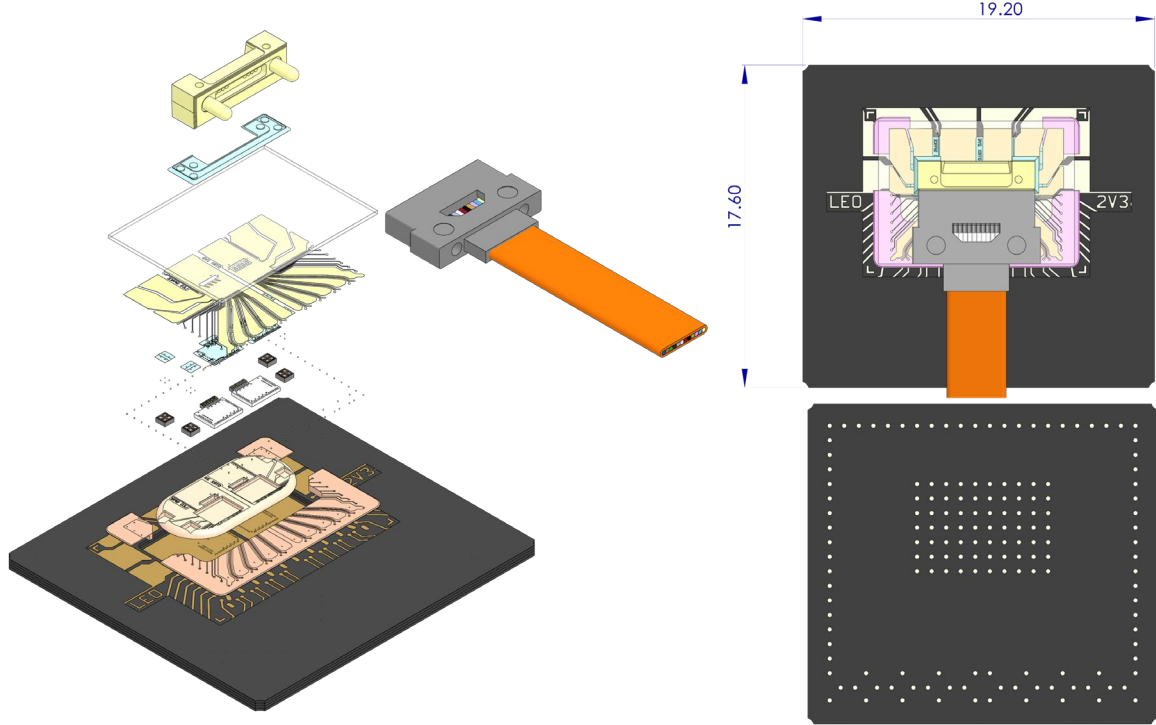


Figure 2. (left): Exploded view of the OTRx assembly showing the ceramic package, transparent chip carrier, active components, optical coupling unit and MT connector, (right) top and bottom view of the OTRx assembly

Figure 2 (right) shows the top and bottom CAD model views of an assembled OTRx. The assembled package measures 17.6 mm × 19.2 mm x 2.84 mm and an occupied host-board area of 3.38 cm². The estimated mass is <1 g. This compact form factor allows the optical engine to be positioned close to the host ASIC or FPGA, so that only a short section of the highest-speed electrical path remains on the PCB.

Table 2. OTRx mechanical form factor.

Parameter	Value
Width	17.6 mm
Length	19.2 mm
Height	2.84 mm
Occupied PCB area	3.38 cm ²
Estimated mass (design estimate)	< 1g

3. OPTICAL ENGINE FABRICATION AND SURFACE-MOUNT ASSEMBLY

3.1 Transparent chip-carrier assembly

The OTRx fabrication begins with automated flip-chip assembly of the optoelectronic and electronic components on the TGCC. The VCSEL and photodiode arrays, the VCSEL-driver and TIA ICs and the decoupling capacitors are mounted

on through a thermo-compression process. This is followed by application of optical and structural underfill on all the components. The transparent substrate enables direct visual inspection of the bonded VCSEL and photodiode arrays through the TGCC, providing an additional in-process verification test during assembly. Figure 3a) shows the top view of the opto-electronic sub-assembly as seen through the TGCC and Figure 3b) shows the detail of the bonded VCSEL array following the application of underfill.

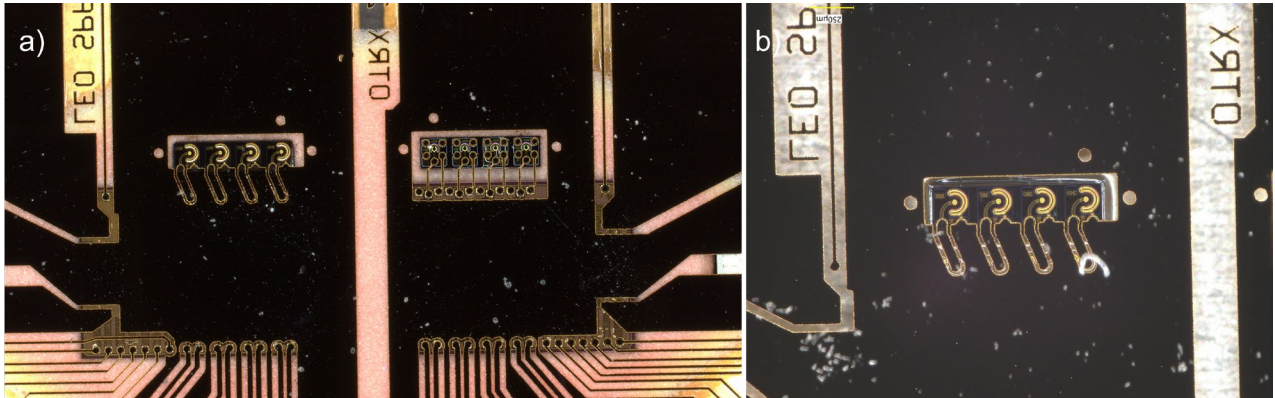


Figure 3. Transparent chip-carrier assembly: (a,b) electronic and optoelectronic die placement and (c,d) detail of the bonded VCSEL and photodiode arrays after optical-underfill application.

The assembled TGCC is subsequently integrated with the ceramic package. The stud-bumped ceramic interface provides the electrical connection between the glass carrier and ceramic substrate. Probe testing is performed before OCU attachment; VCSEL illumination and measurements of OTx and ORx current consumption at this stage are performed as an in-process confirmation that the transmitter/receiver subassembly remains functional after carrier-to-package integration. The OCU is then adhesively bonded to the TGCC with its guide-pin geometry referenced to the optical channels. Following the completion of the packaging process, the mass of the complete assembly was measured at 0.8 g.

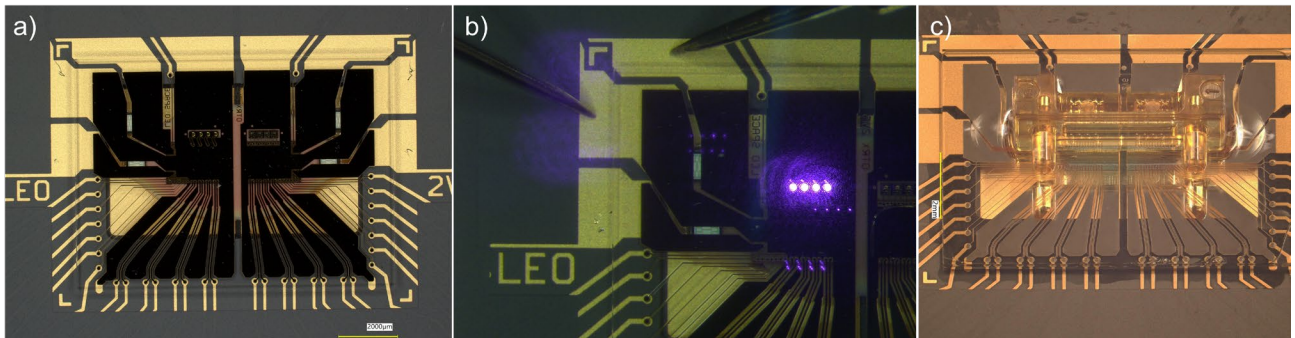


Figure 4. Selected package-assembly steps: (a) transparent chip carrier mounted on the ceramic, (b) in-process probing showing VCSEL illumination and (c) assembly after optical-coupling-unit attachment.

3.2 BGA balling and Pb-free solder reflow

A central objective of the OTRx package is direct board-level solder attachment without an external LGA interposer or socket. The bottom side of the ceramic package therefore implements a 160-position BGA. Balling was performed using a custom stencil and 160 SnBiAg solder balls with 300 μm diameter were attached to the ceramic BGA pads as shown in Figure 6a). The completed optical engine was subsequently reflow-soldered onto a dedicated evaluation PCB using a Pb-free process.

Figure 5b) shows the X-ray inspection image, which was used as a non-destructive check of solder-ball placement and joint formation across the BGA array. Following the inspection, the 12-channel MT connector was mated to the OCU through the guide pins. Figure 5c) shows the complete board-level interface after reflow. Functional characterization was performed after balling, thermal reflow and final PCB attachment so that the reported results include the complete surface-mount assembly sequence.

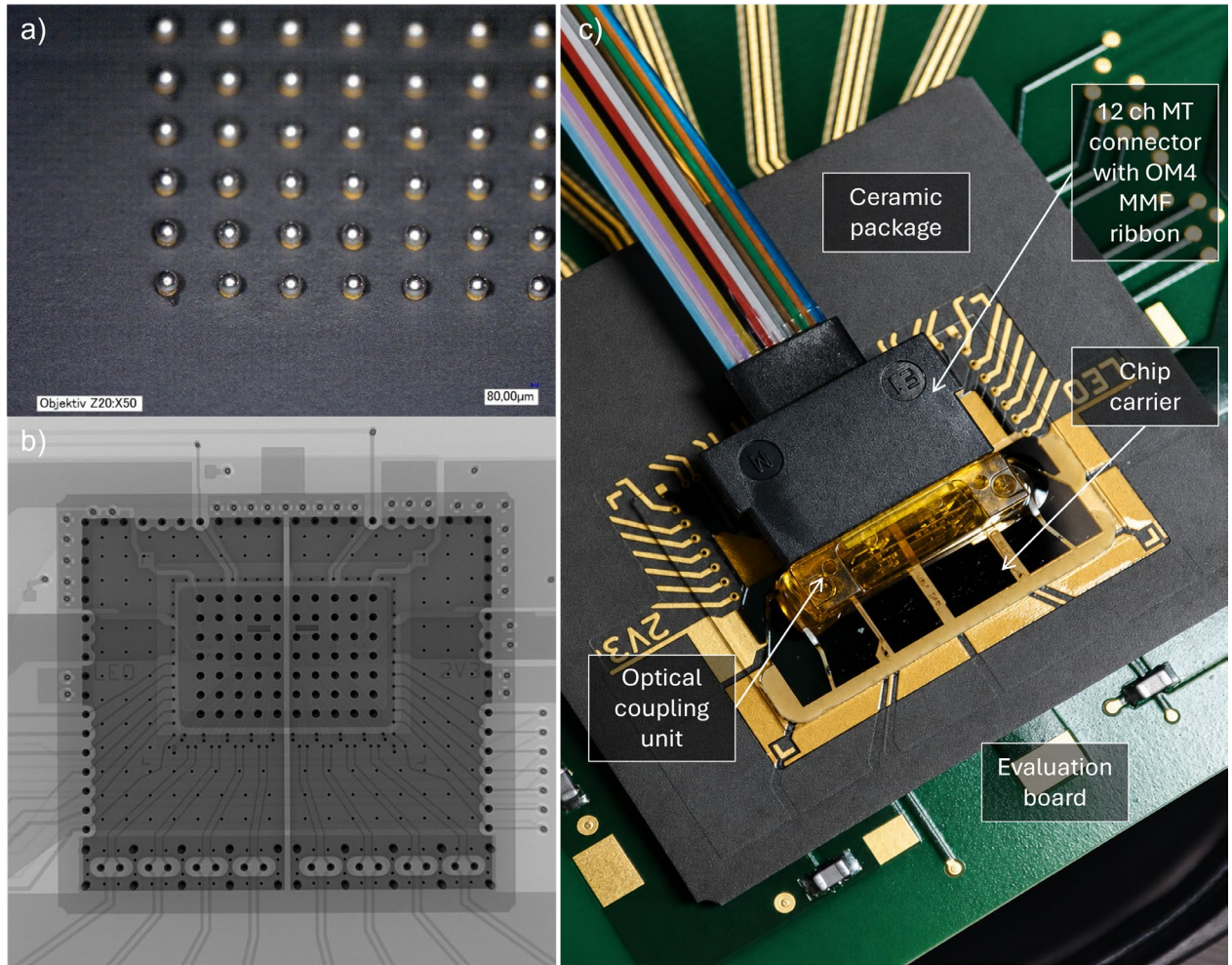


Figure 5. Board-level surface-mount assembly: (a) 300-μm solder balls on the ceramic BGA, (b) X-ray image of the soldered BGA interface and (c) completed OTRx on the evaluation board with a mated MT optical connector.

4. EXPERIMENTAL CHARACTERIZATION

4.1 Test setup

Figure 6 shows the experimental setup used for post-reflow characterization. A bit-error-rate tester (BERT) provides the high-speed electrical data signals applied to the OTRx evaluation board. A DC power supply provides the module supply rails, while an SPI master connected to a host PC through USB, controls the embedded SPI slave interfaces of the driver and receiver ICs. The ribbon fiber array is terminated to an MT ferule, which is connected to an optical fan-out separating the individual fibers. A digital sampling oscilloscope is used with the appropriate optical or electrical input to capture the transmitter optical eye or receiver electrical eye, respectively.

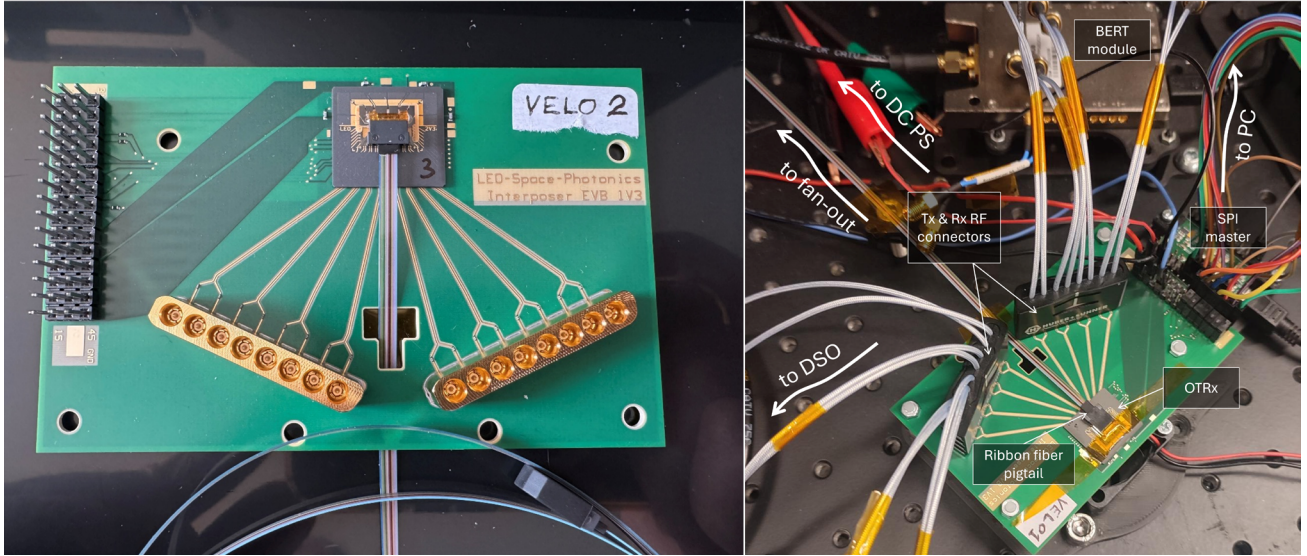
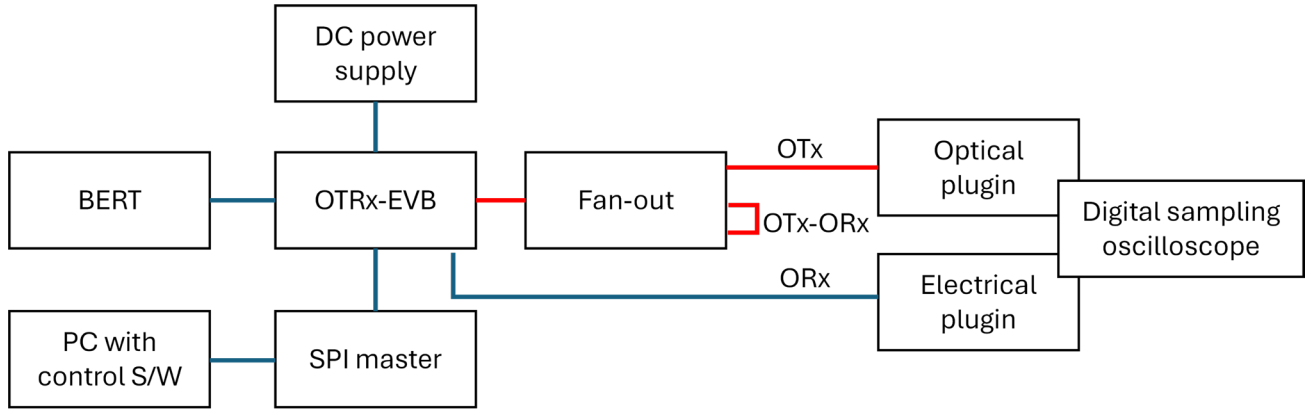


Figure 6. (top) Experimental setup for post-reflow functional and high-speed characterization of the OTRx, (bottom) Evaluation-board implementation and laboratory setup used for the OTRx measurements.

Prior to the high-speed measurements, the monitoring and control functions were tested through the SPI interface. These functional tests confirmed that the assembled device was addressable and that the transmitter and receiver control paths were operational after the complete surface-mount process. High-speed characterization was then performed with eye diagrams and mask benchmarks at 25 and 30 Gb/s.

4.2 25-Gb/s mask-compliance measurements

Figure 7 shows the transmitter optical eye (left) and receiver electrical eye (right) measured at 25 Gb/s. The 100GBASE-SR4 eye mask of the IEEE 100-Gb/s multimode-fiber Ethernet specification [10], was used as a benchmark for signal integrity. The test produced zero mask hits at 10,000 waveforms with margins at 21.9% for the transmitter and 23.3% for the receiver outputs. The transmitter yielded an average optical power of 1.36 mW and an extinction ratio of 5.66 dB.

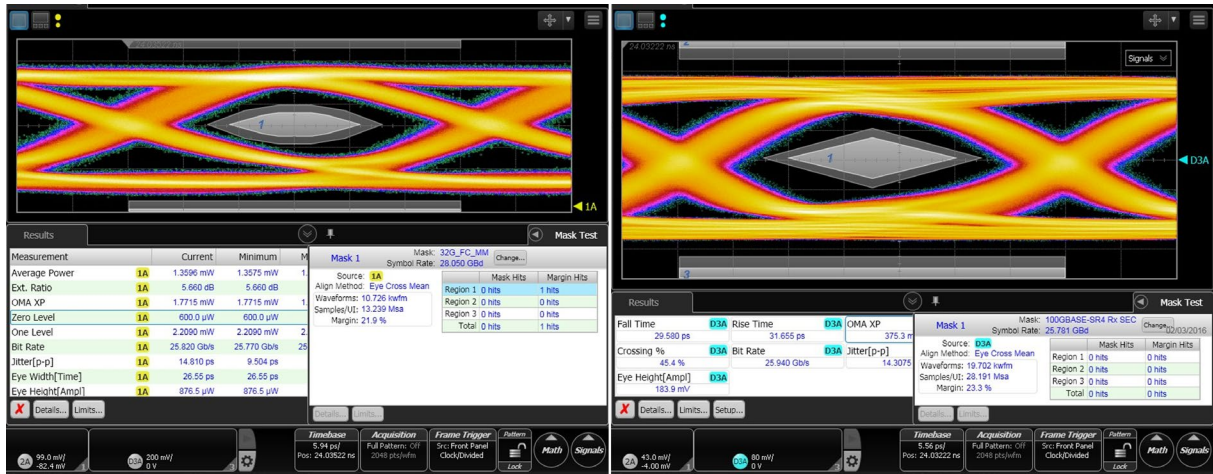


Figure 7. 25-Gb/s 100GBASE-SR4 mask analysis for (left) optical transmitter and (right) electrical receiver

4.3 30-Gb/s operation

The traces in Figure 8 show the measured optical transmitter and electrical receiver eyes at 30 Gb/s. Both data paths exhibit open eyes. The transmitter extinction ratio and the measured average optical output power remain approximately the same. At this lane rate, the four-channel architecture corresponds to $4 \times 30 \text{ Gb/s} = 120 \text{ Gb/s}$ aggregate throughput per direction. Single channel back to back BER tests verified error free operations with $\text{BER} < 1e-12$. Table 3 summarizes the results.

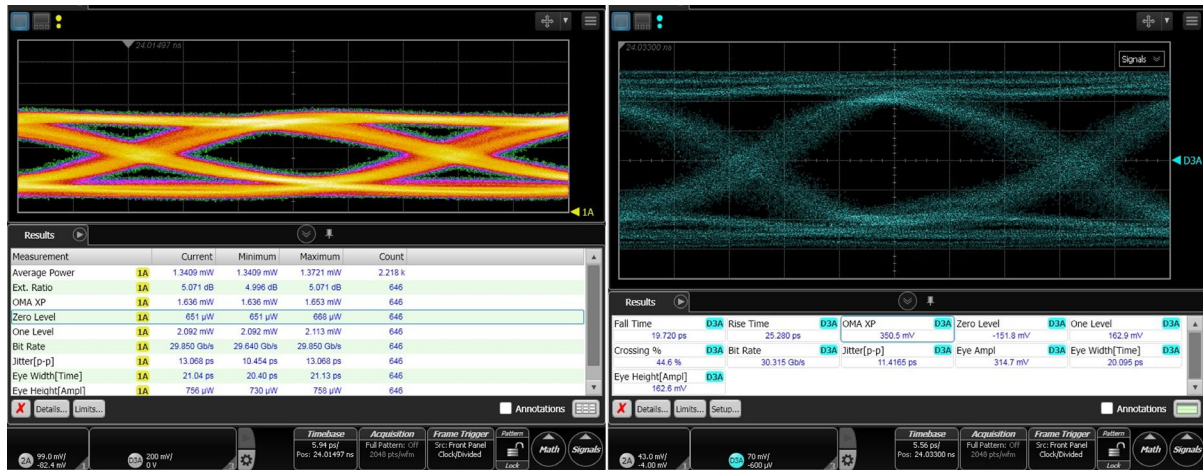


Figure 8. High-speed characterization. Top: 25-Gb/s 100GBASE-SR4 mask analysis for (a) optical transmitter and (b) electrical receiver. Bottom: (c) optical transmitter and (d) electrical receiver eye diagrams at 30 Gb/s.

Table 3. Summary of post-reflow measured results.

Metric	Measured result	Comment
Board-level attachment	160 × 300 μm SnBiAg balls	Reflow-soldered to evaluation PCB; X-ray inspected
25-Gb/s Tx mask test	0 hits; 21.9% margin	>10,000 waveforms
25-Gb/s Rx mask test	0 hits; 23.3% margin	>10,000 waveforms
25-Gb/s Tx optical power	1.36 mW	-
25-Gb/s Tx extinction ratio	5.66 dB	3 dB target
30-Gb/s Tx optical power	1.34 mW	Optical output >1 mW
30-Gb/s Tx extinction ratio	5.07 dB	Electrical receiver output
Aggregate rate	120 Gb/s per direction	4 × 30 Gb/s architecture

5. DISCUSSION

The principal contribution of the demonstrated architecture is a directly soldered near-package optical engine. Compared to previous implementations targeting intra-satellite links, the mid-board architecture reported in [3] used a 17×38.42 module and a COBO-compatible high-speed electrical connector, whereas the commercial hi-rel OTRx product of [4] features a 28.4×14 mm footprint and deploys a dual-compression LGA electrical connector interface. By comparison, the presented OTRx occupies 17.6×19.2 mm, while the electrical connection to the host board is made directly through the BGA.

The demonstrated device sits between conventional pluggable mid-board optics and fully co-packaged optics. Our NPO OTRx approach retains a separately manufacturable and testable optical engine and a removable MT fiber interface, but places the engine adjacent to the host CPU through a soldered BGA. This reduces the length of the highest-speed copper connection without requiring the optical engine to be permanently fiber-pigtailed during board assembly.

The post-reflow results are important because the high-speed characterization was performed only after the optical engine had experienced package balling, Pb-free thermal reflow and final board attachment. The zero-hit eye-mask results at 25 Gb/s and the open Tx/Rx eyes at 30 Gb/s show that the complete assembly sequence is compatible with the intended high-speed data paths. The 30-Gb/s lane rate provides a 120-Gb/s aggregate rate per direction.

6. CONCLUSIONS

A compact 4-Tx/4-Rx VCSEL optical transceiver engine with radiation-hard SiGe BiCMOS electronics has been fabricated and demonstrated in a solder-reflowable BGA package for near-package intra-satellite optical interconnects. The 17.6×19.2 footprint package integrates VCSEL and photodiode arrays, quad driver and TIA ICs, a transparent glass carrier, molded passive coupling optics, a ceramic substrate and a removable MT optical interface. Direct host-board attachment is achieved through a 160-ball, 300- μ m-diameter SnBiAg BGA using a Pb-free reflow process.

Post-reflow X-ray inspection verified the board-level BGA attachment and functional testing at 25 and 30 Gb/s verified high-speed performance. At 25 Gb/s, application of the 100GBASE-SR4 mask as an eye-quality benchmark produced zero hits over more than 10,000 waveforms, with 21.9% and 23.3% margins for the optical Tx and electrical Rx outputs. At 30 Gb/s, both Tx and Rx eyes remained open; the transmitter exhibited approximately 5 dB extinction ratio and optical output above 1 mW. The demonstrated lane rate corresponds to 120 Gb/s aggregate throughput per four-lane direction.

To our knowledge, this is the first reported space-oriented VCSEL transceiver engine to combine radiation-hard SiGe BiCMOS Tx/Rx electronics, a removable MT optical interface and direct board-level BGA solder reflow in a near-package form factor. The architecture removes the separate high-speed LGA/socket interface used by conventional mid-board optics and provides a practical manufacturing path for placing optical I/O close to next-generation satellite ASICs and FPGAs. Future work will focus on module-level radiation and environmental evaluation.

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