The Field-Effect Inverter, a Non-CMOS III-V Semiconductor Unipolar Logic Device in InAs/InGaAs/AlSb/GaSb: From Theory to Proof of Concept

J. J. Hall[1], P. D. Hodgson[1,2] and M. Hayne[1,2]

[1]*Department of Physics, Lancaster University, Lancaster, LA1 4YB, United Kingdom*

[2]*Quinas Technology, Department of Physics, Lancaster University, Lancaster LA1 4YB, United Kingdom*

j.j.hall1@lancaster.ac.uk

It is predicted that by 2030 information technology could consume around 20% of global energy production and emit a similar proportion of global greenhouse gas emissions [1]. Computation is driven by CMOS transistor logic, and with device power density trending upward due to the end of Moore's Law and Dennard Scaling [2], the need for alternative low-power logic devices is evident.

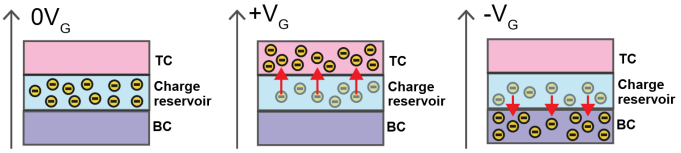

Fig.1 Concept of the FEI shown for electrons. Under zero gate bias (0 V_G) electrons remain in the reservoir. Applying a gate bias (+V_G/-V_G) pulls/pushes electrons into the top/bottom channel respectively, thus achieving the complementary function required for a logic device.

The devices in this work [3] take advantage of the exceptional mobility of electrons in group III-V semiconductors for both "n" and "p"-MOS equivalent operation in a single device, eliminating the compromises and challenges of hole-based conduction in p-MOSFETs. Furthermore, this novel structure, forming a single device field-effect inverter (FEI), halves the number of devices required for logic gates, reducing chip footprint and the number of interconnects. The FEI concept (Fig. 1) consists of two charge-accepting channel layers which sandwich a central electron reservoir. Applying a positive gate bias (+V_G) pulls electrons into the top channel, whilst a negative gate bias (-V_G) pushes electrons into the bottom channel, thus turning one channel on whilst the other remains off: the required complementary function for logic is achieved using only electrons. 1D nextnano++ [4] simulations of the design based on III-V semiconductor alloys with ~6.1-Å lattice constant (InAs/InGaAs/GaSb/AlSb) and analysis of the carrier density integrated over the channel regions (Fig. 2) demonstrates operation. For zero gate bias, the electron density is only ~10^9 cm^{-2}, equivalent to ≤1 carrier in a 300-nm-by-300-nm device. Applying ±1.5 V bias there is ~1,000× increase in the electron density relative to the off-state, and contrast between top and bottom channels is even higher (of the order 10^7). Minimal integrated hole densities are apparent across the entire voltage sweep (~10^{10} cm^{-2}) which, aided by the reduced hole mobility, ensures only electrons are feasible for conduction.

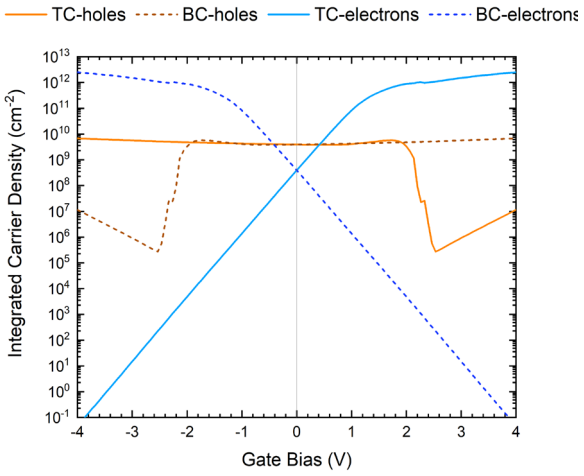

Fig. 2 Integrated charge carrier density calculated from 1D nextnano++ [4] simulation. Top (solid line) and bottom (dashed line) channels are shown for both electrons (blue) and holes (orange). Effective low voltage operation is demonstrated with 2-3 order of magnitude increase in integrated electron density from gate bias 0 V to ±1.5 V. Holes remain at a low background level throughout the voltage sweep.

Work is currently ongoing testing fabricated 10- and 20- µm devices with promising performance allowing demonstration of proof-of-concept FEI devices.

References

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[4] Birner S, Website of nextnano GmbH company (available at: https://www.nextnano.com/)