Gate Materials and Process Variations: Exploring Their Influence on Transport Properties in Silicon MOS Devices

Md. Mamunur Rahman[1], Jonathan Yue Huang[1], Alexandra Dickie[1,2], Steve Yianni[1,2], Kok Wai Chan[1,2], Fay Hudson[1,2],Christopher C. Escott[1,2], Andrea Morello[1], Arne Laucht[1,2], Andre Saraiva[1,2], Andrew S. Dzurak[1,2] and Wee Han Lim[1,2]

[1]*School of Electrical Engineering and Telecommunications, University of New South Wales, Sydney, NSW 2052, Australia*

[2]*Diraq, Sydney, NSW, Australia*

md_mamunur.rahman@unsw.edu.au, a.dzurak@unsw.edu.au, wee.lim@unsw.edu.au

Hall bar carrier mobility and percolation density are two commonly-used metrics to assess the quality of metal-oxide-semiconductor (MOS) interface. By investigating the quantum transport properties of Hall bars, valuable insights can be obtained for fabrication process optimisation and gate materials selection for MOS quantum dot qubit device [1, 2].

In this work, we fabricated a variety of six-terminal Hall bar transistors on high-quality 8-nm SiO_2 gate oxide thermally grown on a high-resistivity natural silicon substrate as shown in Figure 1(a). We varied fabrication parameters such as top gate material, metal deposition process, and lithography type. Throughout this work, the measurements were performed using a standard four-wire lockin technique in a variable temperature insert (VTI) system at $\sim$1.7 K.

Figure 1(b) compares the peak mobility of Al-gated Hall bar device deposited via thermal evaporation or e-beam evaporation while Figure 1(c) shows a comparison between UV photolithography and electron beam lithography at two different acceleration voltages. We observed that device exposure to an electron beam during either gate metal deposition or gate patterning stages leads to the creation of additional negative charge centers in the oxide, resulting in the degradation of electron mobility of the device [3, 4].

In Figure 1(d), we compare the peak mobility of devices made by different gate materials. Aluminium-gated device shows the highest mobility and lowest percolation density (not shown in the figure). A possible explanation is that "Alneal" reduces the Si/SiO_2 interface trap density by atomic hydrogen, which is formed during an oxidation of Al with residual water molecules in the oxide. On the other hand, although being favored for smaller grain size, Pd-gated devices show relatively low mobility. This degradation could be explained by a combined effect of strain-induced modulation on the conduction band of silicon by Pd [5] and an increase of scattering centers by the formation of interface states during the forming gas annealing process [6].

In addition, using titanium(Ti) as an adhesive layer for Pd seems to further reduce the mobility due to the oxygen scavenging of Ti from the underlying SiO_2, reducing it to SiO_x and hence creating defects [2]. Furthermore, introducing an atomic layer deposition (ALD) aluminium oxide between TiPd and SiO_2 creates additional remote scattering sites, which further degrades electron mobility [7].

In summary, we have characterised MOS Hall bar transistors through electrical transport measurements. We found Al achieves the highest mobility when patterned using photolithography and thermal deposition. Further improvements in transport properties can be achieved by reducing scattering centres in the interfaces.

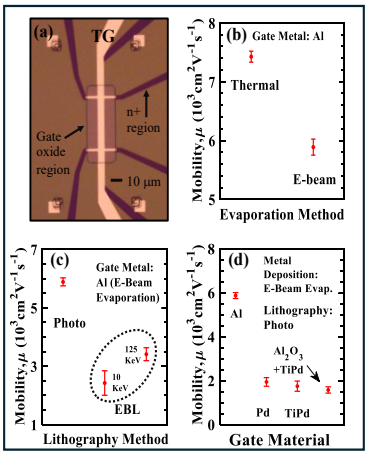

Fig. 1. (a) Optical microscope image of a Hall bar transistor. Comparison of peak mobilities based on (b) metal deposition methods (c) lithography techniques and (d) top gate materials.

References

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