Circuit-level Device Modeling for Analysis of Failure Mechanisms during Selective Erase Operation in 3D CTF memory devices

Sunghwan Cho[1,2], Byoungdeog Choi[3]

[1]*Memory Business, Samsung Electronics Co., Ltd. Hwasung 18448, South Korea*

[2]*Department of Semiconductor and Display Engineering, Sungkyunkwan University, Suwon 16419, South Korea*

[3]*Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 16419, South Korea*

joboss9999@gmail.com

Due to challenges in scaling down feature sizes and addressing limitations such as reliability and interference in planar non-volatile memory devices, 3D charge trapping flash (CTF) memory devices remain the most promising alternative. Nevertheless, 3D CTF memory devices still face limitations in enhancing performance, particularly as the scaling down of flash memory cell size leads to increased cell-to-cell interference. While new methods, such as selective erase operation, have been proposed to effectively utilize memory cells and overcome these limitations, there is still a lack of a suitable framework for analyzing unfamiliar mechanisms using circuit simulation. Therefore, in this study, we have developed a precise circuit-level device model to serve as a framework for analyzing failure mechanisms and optimizing circuit design for the selective erase operation in 3D CTF memory devices. Fig. 1. shows the schematics of hole behavior during conventional erase operation in vertical structure of 3D CTF and 2 erase operational cases described as selective lower WLs erase (SLWE) and selective upper WLs erase (SUWE) in this work. Hole potential should be delivered from p-type well to erasing memory cells through vertical channel with floated body, which result in remarkable difference between SLWE and SUWE operations. Fig. 2 depicts experimental results highlighting the contrasting behavior of holes between SLWE and SUWE. All initially programmed cells in the SLWE case exhibit complete movement of their threshold voltages to below 0V, whereas those in the SUWE case do not. Fig. 3(a) illustrates the variations in WL conditions alongside the equivalent circuit for SPICE modeling. This circuit comprises cylindrical capacitance and voltage-controlled current source components, representing accumulated hole current flowing over the barrier in the channel region and Fowler-Nordheim current for hole erasing through the tunneling oxide layer, respectively. And Fig. 3(b) demonstrates that variations of elevated gate voltages to lower WLs to inhibit the non-erased memory cells can lead to variations in the height of the hole barrier in the channel region of lower WLs and the amount of hole potential delivered to the channel region of upper WLs. Building upon the analyzed mechanism, TCAD and SPICE simulations are performed, as illustrated in Fig. 4. TCAD simulation results reveal that the behaviors of the channel electrostatic potential in the upper WL region vary according to the conditions of lower WLs and the corresponding height of the hole barrier. Moreover, the SPICE simulation results also demonstrate a good fit. The successful alignment of results suggests that the proposed model could serve as a valuable framework for circuit designers to optimize 3D CTF devices.

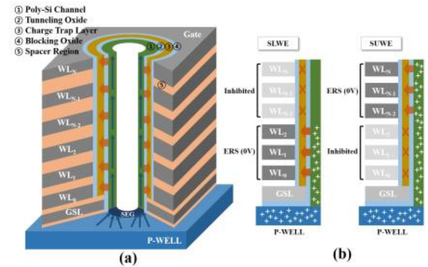

Fig.1 Schematics for erase operation in 3D CTF memory devices

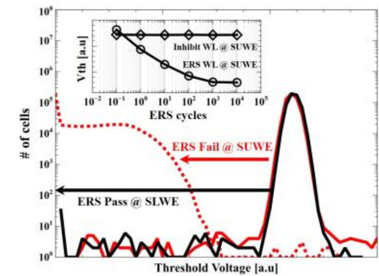

Fig.2 Experimental data for Vth distribution after selective erase.

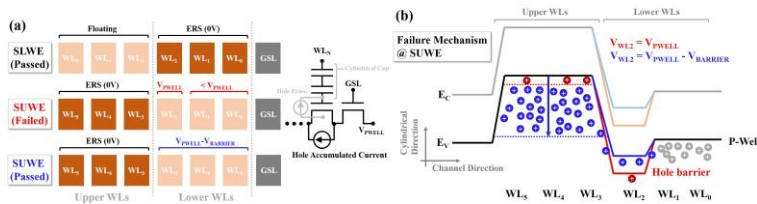

Fig.3 (a) Schematics for variations of WLs (b) The failure mechanism

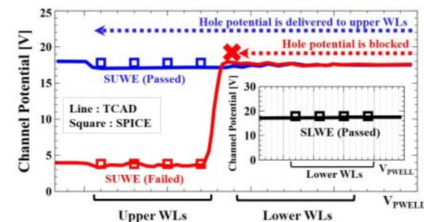

Fig.4 TCAD and SPICE simulation results