Gate-Tunable Negative Differential Resistance in WSe_2/hBN/Graphene Heterostructure

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Negative-differential-resistance (NDR) devices show potential for advanced future computing technologies with very low energy consumption, particularly in the field of multivalued logic computing due to multiple threshold voltages [1]. Here, we report an NDR phenomenon observed in a heterostructure comprised of tungsten diselenide (WSe_2), hexagonal boron nitride (hBN), and graphene in the negative gate voltage regime. In this structure, WSe_2 is employed as a channel material and is aligned with a dielectric hBN, while graphene serves as a floating gate. The investigation of temperature-dependent electrical charge transport using the global gate allows for the identification of the tunneling process within a certain range of gate voltages. In addition, the electrical charge transport measurement demonstrates significant gate-tunable NDR behavior with a maximum peak-to-valley current ratio of 4.7 at room temperature, which improved to 11.8 at a temperature of 77 K. To our best knowledge, this is the unique demonstration of NDR charge transport behavior in a single channel WSe_2 field-effect transistor device. This feature promises many applications such as low-power logical circuits, memory, and high-frequency switching devices [1-4].

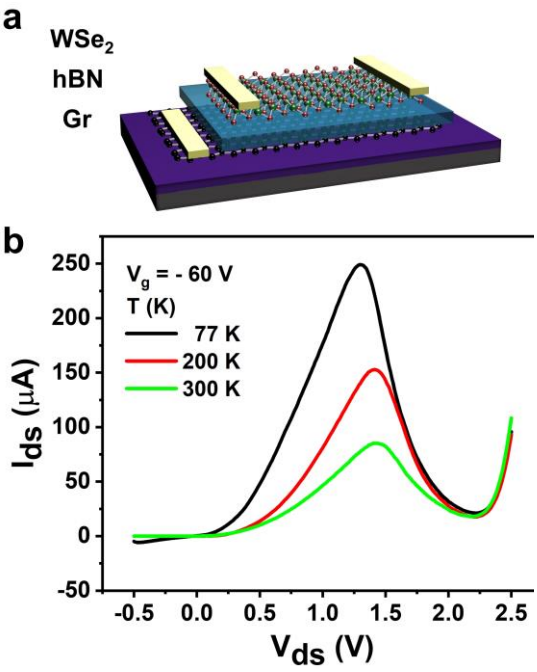

Fig.1. a) Schematic of the WSe_2/hBN/Graphene NDR device. b) At a fixed gate voltage of V_g = - 60 V, the I_{ds}–V_{ds} curves for NDR device at various temperatures ranging from 77 to 300 K.

References

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